

Reg00:	PRATE 10 (20MHz - 40MHz)	SRATE 10 (200 - 400Mbps)	PAREN 0 (Disable)	PWIDTH 000 (10 bits)	Write	Read	Write Both 9258&9257 <input checked="" type="checkbox"/>			
Reg01:	SPREAD 00 (Off)	BANG 0 (Normal)	PDCUR 00 (6.3uA)		Write	Read				
Reg02:	STODIV 1010 (1024)	STOCNT 0000 (0)			Write	Read	<input checked="" type="checkbox"/>			
Reg03:	ETODIV 1010 (1024)	ETOCNT 1001 (9)			Write	Read	<input checked="" type="checkbox"/>			
Reg04:	VEDGE Falling	HEDGE Falling	CKEDGE Rising	CCSPRDIS Enable	LKSHORT Long	DISLEAK Enable	TRN2X Normal	PRBSEN Enable	Write	Read
Reg05:	DEVICEID 1111 100	Write	Read							
							Reg06:	ENDID 1111 111	Write	Read
Reg07:	INTMODE UART	INTEN Enable	FAST 0 - 4Mbps	CTO 100 (64 bits)	BITRATE 00 (95 - 400Kbps)	Write	Read	<input checked="" type="checkbox"/>		
Reg08, 09 (Threshold for number of video parity errors):				Decimal: 16	PATHRLO 0x10	PATHRHI 0x00	Write	Read		
Reg10, 11 (Number of video parity errors):				Decimal: 0	PAERRLO 0x00	PAERRHI 0x00		Read		
Reg12 (PRBS test number of bit errors):				Decimal: 0	PRBSERR 0x00			Read		
Reg13:	DESPERR No	DESFERR No	SERPERR No	SERFERR No	I2CERR No	Read				
Reg14 (Bit length):	Decimal: 37	BITLEN 0x25	Read							

