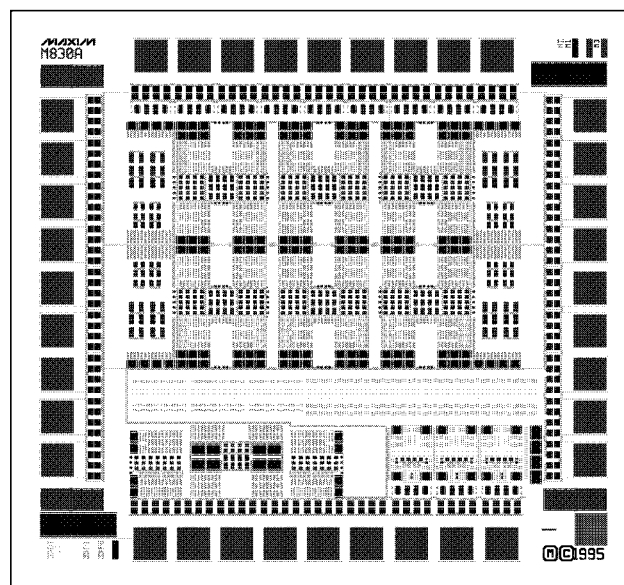


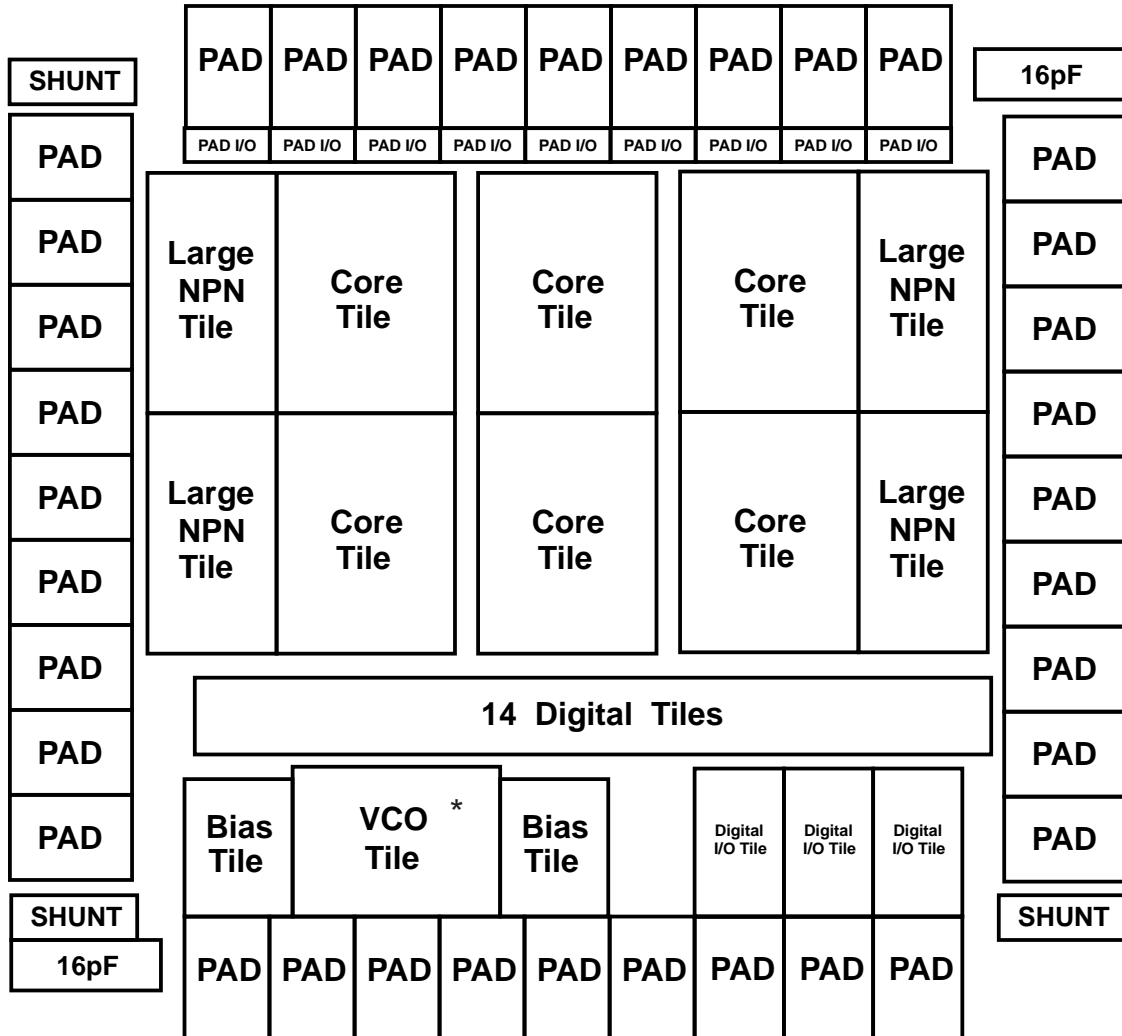
QuickChip 9-60D

The QuickChip 9-60D consists of a 36-pad die, 75 by 70 mils (1.91 x 1.78mm) in size, with 3,790 devices arrayed into different tiles optimized for various analog or digital designs. The analog section consists of 6 core tiles, 4 large NPN tiles, 2 bias tiles, 9 I/O tiles, and 1 tile optimized for use as a VCO with a combined total of 484 NPN transistors, 164 lateral PNP transistors, 114 Schottky diodes, 1,218 resistors (>2.4M Ω total), and 140 capacitors (74pF total). Area is available for custom nichrome resistors in or near each analog tile. The digital section consists of 14 digital tiles (each capable of implementing a clocked master-slave data latch) and 3 digital I/O tiles for both ECL and TTL I/O. Diodes are provided at each bond pad along with 3 prewired supply shunts to protect your design from ESD. Collectively, this QuickChip contains 1,022 NPN transistors, 176 lateral PNP transistors, 426 diodes, 2,008 poly resistors (>6.8M Ω), and 158 capacitors (116pF total). Fabricated on the GST-2 process, QuickChip 9 uses a 3-layer metal interconnect system for high circuit density and low interconnect capacitance. The first and second layers employ a 2.7 μ m pitch metal for signal interconnect while the 5.4 μ m pitch third layer metal is typically used for power supply routing. Unlike many IC processes, GST-2's metal system uses plated gold for high reliability and low resistance. For precision circuits, trimmable resistors are available.

QuickChip 9-60 ARRAY



QuickChip 9-60D TILE LAYOUT



* Tile optimized for use as a VCO may be used for many functions.

