


PKG	8 PIN		14 PIN		16 PIN		
LTR	MIN	MAX	MIN	MAX	MIN	MAX	
A	IN. MM	0.053 1.35	0.069 1.75	0.053 1.35	0.069 1.75	0.053 1.35	0.069 1.75
A1	IN. MM	0.004 0.10	0.010 0.25	0.004 0.10	0.010 0.25	0.004 0.10	0.010 0.25
A2	IN. MM	0.048 1.22	0.062 1.57	0.048 1.22	0.062 1.57	0.048 1.22	0.062 1.57
b	IN. MM	0.012 0.30	0.020 0.51	0.012 0.30	0.020 0.51	0.012 0.30	0.020 0.51
C	IN. MM	0.007 0.18	0.011 0.28	0.007 0.18	0.011 0.28	0.007 0.18	0.011 0.28
D	IN. MM	0.188 4.78	0.196 4.98	0.337 8.56	0.344 8.74	0.386 9.80	0.393 9.98
e	IN. MM	.050 BSC 1.27 BSC		.050 BSC 1.27 BSC		.050 BSC 1.27 BSC	
E1	IN. MM	0.150 3.81	0.158 4.01	0.150 3.81	0.158 4.01	0.150 3.81	0.158 4.01
H	IN. MM	0.230 5.84	0.244 6.20	0.230 5.84	0.244 6.20	0.230 5.84	0.244 6.20
L	IN. MM	0.016 0.41	0.050 1.27	0.016 0.41	0.050 1.27	0.016 0.41	0.050 1.27
theta		0°	8°	0°	8°	0°	8°

THE CHAMFER ON THE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A TERMINAL 1 IDENTIFIER MUST BE POSITIONED SO THAT 1/2 OR MORE OF IT'S AREA IS CONTAINED IN THE HATCHED ZONE.

SIGNATURE		DATE	 Dallas Semiconductor			
DOC. CONTROL:						
ENGR. MGR:			TITLE			
MFG. ENGR:			PACKAGE OUTLINE .150" SOIC 8,14&16 LD.			
CHECKED BY:			SIZE	FSCM NO	PART NO.	REV
DRAWN BY:			A			B
DO NOT SCALE DWG.			SCALE N/A		SHEET 1 OF 1	