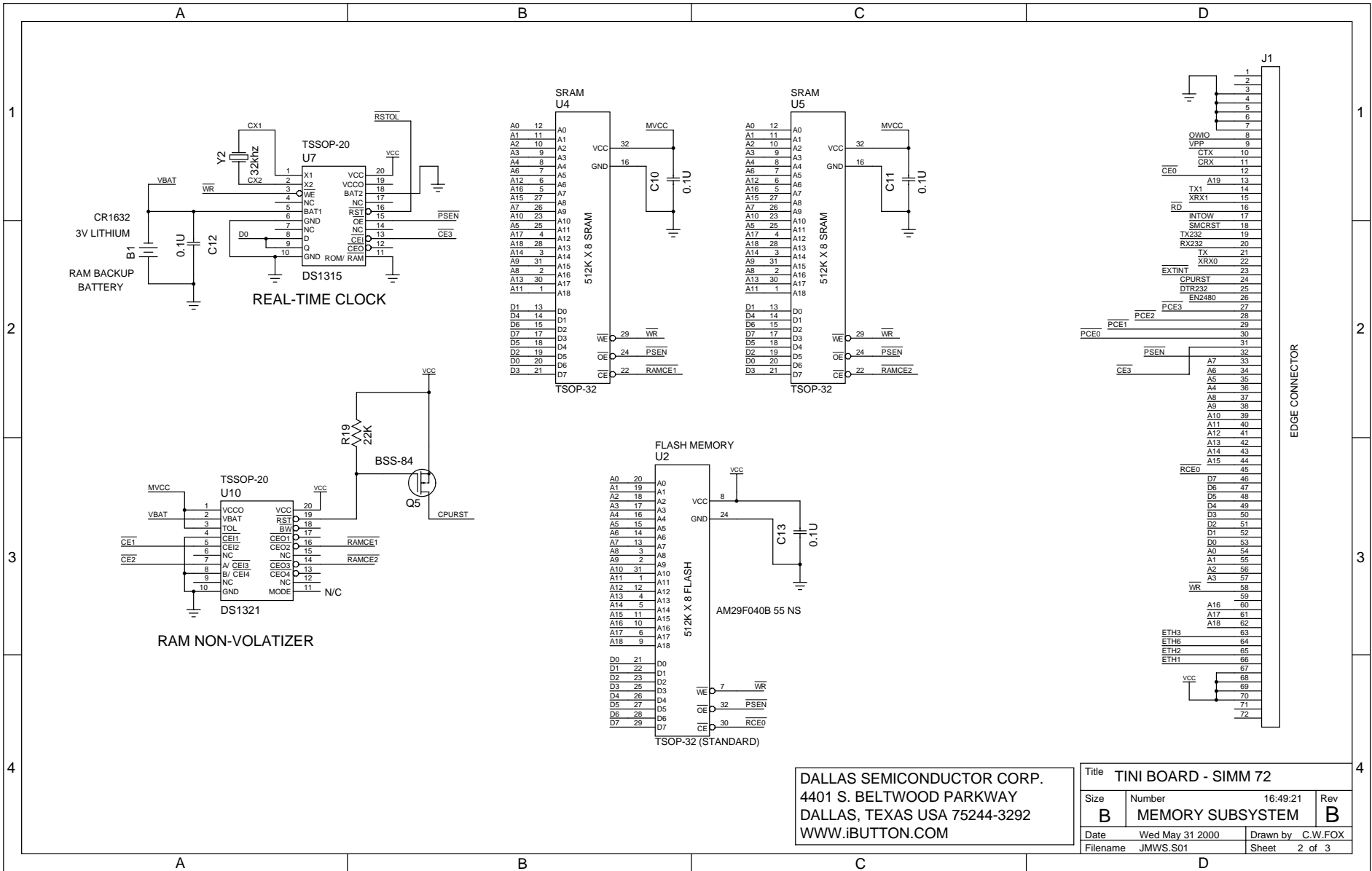


DALLAS SEMICONDUCTOR CORP.
 4401 S. BELTWOOD PARKWAY
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REV G SCHEMATIC IS THE SAME AS REV H.

Title TINI BOARD - SIMM 72			
Size B	Number CPU AND CONTROL	16:49:21	Rev B
Date	Wed May 31 2000	Drawn by	C.W.FOX
Filename	JMWS.S01	Sheet	1 of 3



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Title TINI BOARD - SIMM 72			
Size	Number	16:49:21	Rev
B	MEMORY SUBSYSTEM		B
Date	Wed May 31 2000	Drawn by	C.W.FOX
Filename	JMWS.S01	Sheet	2 of 3

Dallas Semiconductor

TINI Board
(72 Pin SIMM Format)

Board Edge Connector
Pin Out Data

****PRELIMINARY****

72 Pin SIMM Edge Connector Pinout -

Pin	Name	Signal Description	Level	Note:	Requirements (See Notes)
1, 2	-	N/C	-		
3-5	GND	Ground	PWR		
6-7	USB	Future USB Port Pins	C/T		
8	OWIO	Primary 1-Wire port data	C/T		
9	VPP	+12V VPP input to DS2480	PWR	Note 2	Connect to VCC if not used
10	CTX	CAN bus TX line or port pin	C/T		
11	CRX	CAN bus RX line or port pin	C/T		
12	*CE0	CPU Chip Enable 0	C/T	Note 1	Connect to *RCE0
13	A19	CPU Address Line A19	C/T	Note 7	
14	TX1	Secondary Serial Port Output	C/T		
15	RX1	Secondary Serial Port Input	C/T		
16	*RD	CPU Read Strobe	C/T	Note 7	
17	INTOW	Internal One Wire Bus	C/T	Note 4	Master Clear
18	SMCRST	Peripheral reset from CPU	C/T		
19	TX232	Primary Serial Port Output	232		
20	RX232	Primary Serial Port Input	232		
21	TX	Primary Serial Port Output	C/T		
22	RX	Primary Serial Port Input	C/T		
23	*INT	CPU Interrupt Input	C/T		
24	CPURST	CPU Reset Input	C/T	Note 5	Pull high to invoke CPU reset
25	DTR232	RS232 CPU Reset Input	232	Note 6	Connects to DTR line
26	EN2480	On-board DS2480 enable	C/T		Ground to disable DS2480
27	*PCE3	Peripheral Chip Enable 3 from CPU	C/T	Note 7	
28	*PCE2	Peripheral Chip Enable 2 from CPU	C/T	Note 7	
29	*PCE1	Peripheral Chip Enable 1 from CPU	C/T	Note 7	
30	*PCE0	Peripheral Chip Enable 0 from CPU	C/T	Note 7	
31	*CE3	Chip Enable 3 from CPU	C/T	Note 7	
32	*PSEN	Program Store Enable from CPU	C/T	Note 7	
33	A7	CPU Address Line	C/T	Note 7	
34	A6	CPU Address Line	C/T	Note 7	
35	A5	CPU Address Line	C/T	Note 7	
36	A4	CPU Address Line	C/T	Note 7	
37	A8	CPU Address Line	C/T	Note 7	
38	A9	CPU Address Line	C/T	Note 7	
39	A10	CPU Address Line	C/T	Note 7	
40	A11	CPU Address Line	C/T	Note 7	
41	A12	CPU Address Line	C/T	Note 7	
42	A13	CPU Address Line	C/T	Note 7	
43	A14	CPU Address Line	C/T	Note 7	
44	A15	CPU Address Line	C/T	Note 7	
45	*RCE0	CE0 return to on-board Flash ROM	C/T	Note 1	Connect to *CE0 (See notes)
46	D7	CPU Data Bus Line	C/T	Note 7	Bi-directional
47	D6	CPU Data Bus Line	C/T	Note 7	Bi-directional
48	D5	CPU Data Bus Line	C/T	Note 7	Bi-directional
49	D4	CPU Data Bus Line	C/T	Note 7	Bi-directional
50	D3	CPU Data Bus Line	C/T	Note 7	Bi-directional
51	D2	CPU Data Bus Line	C/T	Note 7	Bi-directional
52	D1	CPU Data Bus Line	C/T	Note 7	Bi-directional
53	D0	CPU Data Bus Line	C/T	Note 7	Bi-directional

54	A0	CPU Address Line	C/T	Note 7	
55	A1	CPU Address Line	C/T	Note 7	
56	A2	CPU Address Line	C/T	Note 7	
57	A3	CPU Address Line	C/T	Note 7	
58	*WR	CPU Write Strobe	C/T	Note 7	
59		N/C			
60	A16	CPU Address Line	C/T	Note 7	
61	A17	CPU Address Line	C/T	Note 7	
62	A18	CPU Address Line	C/T	Note 7	
63	ETH3	Ethernet 10-Base-T Connection	ETH		
64	ETH6	Ethernet 10-Base-T Connection	ETH		
65	ETH2	Ethernet 10-Base-T Connection	ETH		
66	ETH1	Ethernet 10-Base-T Connection	ETH		
67-70	Vcc	+5 Volts DC +/- 5% @ 250ma max	PWR	Note 3	TINI Board power supply
71,72	-	N/C	-		

Notes:

1. To execute from the on-board Flash ROM, connect *CE0 (Pin 12) to *RCE0 (Pin 45). If an external boot-up memory is provided, *RCE0 must be pulled high (Vcc) to disable the on-board Flash ROM or data bus interference could occur. Logic in the *CE0 to *RCE0 path must take care to present minimal delay (<10ns) to the CE0 signal.
2. Pin 9 (Vpp) may be connected to +12 VDC to allow EPROM programming with the on-board DS2480. If not use in this manner, Pin 9 (Vpp) must be connected to the Vcc.
3. TINI Board power consumption is rated at no more than 250ma as of this writing. However, changes are being made to reduce this to below 200ma in the next revision.
4. The Internal One Wire Bus (INTOW) is a micro-controller port pin that drives the CPU status LED and links to the board One Wire Serial Number/MAC Address memory device. Other One Wire devices may be connected to this bus in the future to convey configuration data to the TINI board. If this bus is shorted to ground (low) during system boot-up, a Master Clear will be invoked.
5. CPURST must be taken high (Vcc) and then released to cause a TINI Board reset. An active state on the RS232 level DTR line (Pin 25) will also take this line high. This line is pulled down through 10K ohms on-board.
6. The RS232 level DTR control line is used to invoke a TINI Board reset when asserted. This is to facilitate loaders and diagnostic equipment that must invoke a reset of the board to gain control of the system. This line is pulled to -8 volts via 22K ohms and has a 22000 pf capacitor filter to prevent cross-talk on an open DTR conductor from causing spurious TINI board resets if this function is not used.
7. Address bus, data bus and strobe lines are subject to strict loading limitations. Exceeding these limits can cause erratic system operation with on-board as well as off-board resources. Be sure to buffer any signals that will be heavily loaded off-board. Always adhere to the design specifications to assure reliable system operation.