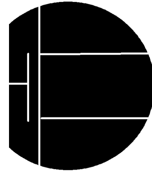

DALLAS
SEMICONDUCTOR

RELIABILITY MONITOR PROGRAM

FIRST QUARTER 1996 REPORT

This report has been prepared by:

Dallas Semiconductor
Quality Assurance Department
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DALLAS SEMICONDUCTOR

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RELIABILITY MONITOR PROGRAM

Overview

Dallas Semiconductor monitors the reliability of devices representative of those shipped from production to ensure that failure rates are met on a continuing basis. Through the Reliability Monitor Program (RMP), the reliability of key wafer fab and assembly processes are monitored for different device families under accelerated conditions. Sample sizes vary but are typically 200+ devices per family divided between a variety of environmental stresses. The results from the RMP are reported quarterly.

The RMP has been established on twelve product families which are listed with devices and sampling plans in Table 1. Devices from substitute assembly sites are used when devices from the preferred assembly sites are not available. Exceptions to the sampling plan, for the current quarter, are shown below:

Sample Period	Product	Assembly Site	Alternate Site Sampled	Comments
January	DS1232	Hyundai	Anam, K.	
January	DS12885	Hyundai	Anam, PI.	
January	DS2165	Anam, PI.	Hyundai	
February	DS1232	Anam, PI.	None	Not Available
February	DS1585	Hyundai	None	Not Available
February	DS1669	Omedata	None	Not Available
March	DS232	Omedata	Anam, PI.	
March	DS12885	Hyundai	Anam, K.	

All failures from the RMP are verified then analyzed for cause of failure. The results of this analysis are used to establish corrective actions to eliminate the failure mechanisms found.

Data Summaries
for latest quarter
Reliability Monitor Program

Data is published quarterly by the Dallas Semiconductor Quality Assurance Department. The results of testing in the latest quarter are summarized in attachment A. Failure rate calculations included in each page of the summary are for that monitor date only. Cumulative results for operating life and infant mortality are included in the graphs of the summaries in attachment B.

Attachment B includes historical data for most products and stresses, in table form, from the previous twelve months. This is followed by infant/operating life data which is graphed to show trends in reliability. The graphs are generated using historical CHI-SQ summary statistics at the 60% confidence level. Dallas Semiconductor uses cumulative device hours and calculates the failure rate at use conditions (55°C and 5.5V) for each failure mechanism separately using the activation energy and the Beta of that mechanism, if known. An activation energy of 0.7ev and a Beta of 1.0 are used whenever actual failure mechanisms or their activation energies / Betas are unknown. Failure rates are then summed assuming no interaction between differing failure mechanisms. Infant mortality failures are not included in the long term reliability calculations but are graphed separately. Binomial probability statistics at the 90% confidence level are used for this calculation. The cumulative results for both infant mortality and long term reliability are rolled according to the last six data points and failures from the different read points are averaged according to the rule of 21's; that is, the latest data is waited as 6/21's, the previous period 5/21's, etc. Weighted sums are then multiplied by the number of read points before final results are calculated and plotted. This technique tends to exacerbate the more recent failures but at the same time will more appropriately reflect trends.

Attachment C summarizes the corrective actions to problems / failures which were found in the Reliability Monitor Program and which are still active.

Stress Tests
used for
Reliability Monitor Program

Preconditioning Stresses

Preconditioning stresses are used to monitor the contribution that post assembly environment has on the reliability of devices. Two types of preconditioning stress are used at Dallas Semiconductor. The first is the Belcore preconditioning stress, specification no. TR-TSY-000357, which is used for all PDIP Telecom products and consists of 10 cycles of -55°C / +125°C temperature cycling and 48 hours of 7.0 volt, 125°C dynamic operating life prior to splitting the lot into the various stress groups. The second preconditioning stress is Dallas Semiconductor's own preconditioning stress used to monitor all package types determined to be moisture sensitive. These package types, at this time, include SOIC's, QFP's, TSSOP's and PLCC's. This stress consists of a single

pass of vapor phase reflow prior to splitting the lot into the various stress groups which includes an ultrasound test to look for package cracks and die surface delamination from the package.

Operating Life and High Voltage Life (Burn-in)
These stresses simulate typical device performance at elevated temperatures and nominal (Operating Life), as well as higher than nominal (High Voltage Life) voltages and, then, use the relationship between temperature, voltage, and time to derate to use conditions. The chamber where devices are stressed consists of an oven capable of withstanding the accelerated temperature. Devices are biased via life test boards programmed to provide dynamic exercising of the circuit. Devices are electrically tested at various read points in order to determine under these accelerated conditions how the device might perform in infant life and long term life. Devices are required to satisfy all data sheet specifications over full voltage and temperature ranges at all read points, independent of the type of stress. Operating Life and High Voltage Life are performed on integrated circuits only. Usual conditions are 125°C, 5.5 volts, and 125°C, 7.0 volts, for 1000 hours.

Storage Life
The purpose of this stress is to accelerate aging of product under storage conditions and is used for Telecom, EPROM, & EEPROM integrated circuits. Typical conditions are 150°C for 1000 hours with no bias applied. The stress chamber is an oven capable of withstanding the high temperatures of the storage condition. Some battery backed modules are initially subjected to storage life as a preconditioning stress (48 hours), but under a reduced temperature of 85°C due to the thermal limitations of the lithium battery. Other battery backed products are subjected to storage life for 1000 hours at temperatures of 70°C or 85°C. Devices are electrically tested at various read points in order to evaluate the performance of the product over time.

Temperature Cycle
The object of this stress is to simulate the conditions of temperature change due to power-up / power-down sequences which devices are normally subjected to under use conditions. This stress will reveal weaknesses in design related to mismatch of thermal characteristics in the package materials and in the die to package relationships. Typical conditions vary with product. For integrated circuits, -55°C to +125°C (no bias) for 1000 cycles, is the usual stress. Thermal transition and soak times conform to MIL-STD-883, Method 1010, Condition B. For modules or other battery backed products the stress range is reduced to 0°C to +70°C or -40°C to +85°C (no bias). Devices are electrically tested at each read point to full data sheet specifications.

Temperature Humidity (Biased and Unbiased)
The purpose of this stress is to determine the performance of products when subjected to a humid, high temperature environment. Standard, industry accepted, stress tests have been developed which are designed to simulate field conditions over the life time of the product. These standard stresses are 120°C / 85% relative humidity for 100 hours (HAST) or 85°C / 85% relative humidity for 959 hours. Both stresses are performed with maximum alternating bias, in this case, 5.5 and 0.0 volts, which provides an opportunity for electrochemical corrosion. Devices are configured for lowest power dissipation to reduce internal heating and subsequent reduction in internal humidity. This stress examines the integrity of the encapsulated device and the quality of the surface passivation to prevent corrosion on integrated circuits. The stress is used for both

modules and integrated circuits. Other battery backed products are subjected to moisture soak consisting of 60°C and 90% relative humidity without external bias. Autoclave testing consists of 120°C and 2 Atmospheres of pressure without bias for 96 hours and is performed on integrated circuits. Devices are electrically tested at all read points.

Package Integrity

The purpose of the package integrity testing is to verify the incoming quality of our assembly suppliers by performing package tests to currently qualified specifications. Physical dimensions and Solderability of modules, and Ultrasound of surface mount packages are performed and reported as part of the RMP. Physical dimensions, Lead integrity, Solderability, X-ray views, X-ray fluorescence, and external visual tests are performed on integrated circuits by Incoming Quality Control on a weekly monitor basis. These IQC monitors include all package types per assembly sites for product received each week.

Ultrasound testing is used in lieu of Dye Penetration Tests. Ultrasound testing is a sensitive technique that can delineate package voids and internal interface separations and cracks. All of this can be done nondestructively. No internal crack nor die surface delamination is allowed in this inspection.

External physical dimensions are measured per MIL-STD-883, Method 2016. The measurements are compared to the currently active specification for the device in test. Failure can result in lot rejection, supplier disqualification, or correction to the specification.

Solderability is tested per MIL-STD-883, Method 2003. All leads are dipped on a sample size of three units, then 24 leads on the three devices are inspected. Type R Flux is used. Accept criteria is 95% coverage. For the Modules, type RMA Flux is used and acceptance criteria is 90% coverage.

Lead Integrity is tested to MIL-STD-883, Method 2004, test condition B2. Twenty-four leads are tested on a sample size of six units. For Plastic dual-in-line packages, a 15° bend is used.

Radiography (X-ray) is performed per MIL-STD-883, Method 2012. Top and side views of x-rays are recorded on film.

X-ray fluorescence is performed to verify plating thickness and composition.

External visual is performed per an internal DSC specification (27-03510-000) in order to verify the correct marking and external package integrity.

Summary

A summary of all stress tests used in the Reliability Monitor and the sample sizes used with each test is shown in Tables 2, 3, 4 and 5.