DALLAS
SEMICONDUCTOR

# RELIABILITY MONITOR PROGRAM

# THIRD QUARTER 2000 REPORT

**This report has been prepared by:**

**Dallas Semiconductor**
**Quality Assurance Department**
**010/20/00**

DALLAS
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# RELIABILITY MONITOR PROGRAM

## Overview

Dallas Semiconductor monitors the reliability of devices representative of those shipped from production to ensure that failure rates are met on a continuing basis. Through the Reliability Monitor Program (RMP), the reliability of key wafer fab and assembly processes are monitored for different device families under accelerated conditions. Sample sizes vary but are typically 200+ devices per family divided between a variety of environmental stresses. The results from the RMP are reported quarterly.

The RMP has been established on twelve product families which are found in the RMP DEVICE SAMPLING PLAN section of this report. The wafer fab processes sampled, the devices covered by this sample, and the vehicle used to sample these processes are found in the RMP PROCESS SAMPLING PLAN. Devices from substitute assembly sites are used when devices from the preferred assembly sites are not available.

All failures from the RMP are verified then analyzed for cause of failure. The results of this analysis are used to establish corrective actions to eliminate the failure mechanisms found.

## Data Summaries
## for latest quarter
## Reliability Monitor Program

Data is published quarterly by the Dallas Semiconductor Quality Assurance Department. The results of testing in the latest quarter are divided and can be found in the IC RELIABILITY DATA or the MODULE RELIABILITY DATA sections depending on the technology type. Failure rate calculations included in IC RELIABILITY DATA of the report are for that monitor date only.

The PROCESS RELIABILITY SUMMARY includes historical data for IC products and Operating Life Stresses, in table form, from the previous quarter. Data is organized by design technology. Dallas Semiconductor uses cumulative device hours and calculates the failure rate at use conditions (55°C and 5.5V) for each failure mechanism separately using the activation energy and the voltage acceleration Beta of that mechanism, if known. An activation energy of 0.7ev and a Beta of 1.0 are used whenever actual failure mechanisms or their activation energies / Betas are unknown. These are conservative industry standards. The ASSEMBLY/PACKAGE RELIABILITY SUMMARY section summarizes the assembly/package stresses for the quarter. Data in this section is organized by stress type, assembly site, and package technology.

## Corrective Action Data

This report has included a corrective action to failure mechanisms identified in failure analysis of RMP failures. Results of this analysis and corrective action are shown at the bottom of each device summary in the RELIABILITY DATA section of the report. Note that not all failures have been submitted to failure analysis but are in the process of being characterized or resolved. Failures which are not the result of device or process performance are removed from the RMP.

## Outgoing PPM Estimate

Estimates of the Outgoing PPM rate for Dallas Semiconductor product have been added to the RMP report in an effort to enhance its usefulness. The purpose of this data is to give a best estimate of what a customer might expect to see in using the Dallas Semiconductor products. The data being reported is from the final QC lot acceptance test and will reflect both the Visual/Mechanical and Electrical results.

Since there is some rescreening of rejected lots after the QC lot acceptance tests, the raw data requires some adjustment to better reflect what results might be expected by the end customer. The calculation method we have chosen to deal with this issue involves removing the effects of the lots that have a very low probability of shipment to

the customer. Therefore, any lot that had three more rejects than the accept number of the sampling plan has been removed from the data set. All of the remaining data is summarized with the total rejects divided by the total sample size to give our best estimate of what the actual PPM rate past the QC lot acceptance test will be.

OUTGOING QUALITY SUMMARY reports the Outgoing Quality, Visual and Electrical PPM, for the last several quarters.

## Stress Tests included in the Reliability Monitor Program

### Preconditioning Stresses

Preconditioning stresses are used to monitor the contribution that post assembly environment has on the reliability of devices. Two types of preconditioning stress are used at Dallas Semiconductor. The first is the Belcore preconditioning stress, specification no. TR-TSY-000357, which is used for all PDIP Telecom products and consists of 10 cycles of -55°C / +125°C temperature cycling and 48 hours of 7.0 volt, 125°C dynamic infant life prior to splitting the lot into the various stress groups. The second preconditioning stress is per J-STD-020 and is used to monitor all package types determined to be moisture sensitive. These package types, at this time, include SOIC's, QFP's, TSSOP's and PLCC's. This stress consists of a bake, moisture soak, and three passes of vapor phase reflow prior to splitting the lot into the various stress groups which includes an ultrasound test to look for package cracks and die surface delamination from the package.

### Operating Life and High Voltage Life (Burn-in)

These stresses simulate typical device performance at elevated temperatures and nominal (Operating Life), as well as higher than nominal (High Voltage Life) voltages and, then, use the relationship between temperature, voltage, and time to derate to use conditions. The chamber where devices are stressed consists of an oven capable of withstanding the accelerated temperature. Devices are biased via life test boards programmed to provide dynamic exercising of the circuit. Devices are electrically tested at various read points in order to determine under these accelerated conditions how the device might perform in infant life and long term life. Devices are required to satisfy all data sheet specifications over full voltage and temperature ranges at all read points, independent of the type of stress. Operating life and high voltage life are performed on integrated circuits only. Usual conditions are 125°C, 5.5 volts, and 125°C, 7.0 or 6.0 volts, for 1000 hours.

### Storage Life

The purpose of this stress is to accelerate aging of product under storage conditions and is used for Telecom, EPROM, & EEPROM integrated circuits. Typical conditions are

150°C for 1000 hours with no bias applied. The stress chamber is an oven capable of withstanding the high temperatures of the storage condition. Some battery backed modules are initially subjected to storage life as a preconditioning stress (48 hours), but under a reduced temperature of 85°C due to the thermal limitations of the lithium battery. Other battery backed products are subjected to storage life for 1000 hours at temperatures of 70°C or 85°C. Devices are electrically tested at various read points in order to evaluate the performance of the product over time.

**Temperature Cycle**

The object of this stress is to simulate the conditions of temperature change due to power-up / power-down sequences which devices are normally subjected to under use conditions. This stress will reveal weaknesses in design related to mismatch of thermal characteristics in the package materials and in the die to package relationships. Typical conditions vary with product. For integrated circuits, -55°C to +125°C (no bias) for 1000 cycles, is the usual stress. Thermal transition and soak times conform to MIL-STD-883, Method 1010, Condition B. For modules or other battery backed products the stress range is reduced to 0°C to +70°C or -40°C to +85°C (no bias). Devices are electrically tested at each read point to full data sheet specifications.

**Temperature Humidity (Biased and Unbiased)**

The purpose of this stress is to determine the performance of products when subjected to a humid, high temperature environment. Standard, industry accepted, stress tests have been developed which are designed to simulate field conditions over the life time of the product. These standard stresses are 120°C / 85% relative humidity for 100 hours (HAST) or 85°C / 85% relative humidity for 959 hours. Both stresses are performed with maximum alternating bias, in this case, 5.5 and 0.0 volts, which provides an opportunity for electrochemical corrosion. Devices are configured for lowest power dissipation to reduce internal heating and subsequent reduction in internal humidity. This stress examines the integrity of the encapsulated device and the quality of the surface passivation to prevent corrosion on integrated circuits. The stress is used for both modules and integrated circuits. Other battery backed products are subjected to moisture soak consisting of 60°C and 90% relative humidity without external bias. Autoclave testing consists of 120°C and 2 Atmospheres of pressure without bias for 96 hours and is performed on integrated circuits. Devices are electrically tested at all read points.

**Package Integrity**

The purpose of the package integrity testing is to verify the incoming quality of our assembly suppliers by performing package tests to currently qualified specifications. Physical dimensions and Solderability of modules, and Ultrasound of surface mount packages are performed and reported as part of the RMP. Physical dimensions, Lead integrity, Solderability, X-ray views, X-ray fluorescence, and external visual tests are performed on integrated circuits by Incoming Quality Control on a weekly monitor basis. These IQC monitors include all package types per assembly sites for product received each week.

Ultrasound testing is used in lieu of Dye Penetration Tests. Ultrasound testing is a sensitive technique that can delineate package voids and internal interface separations and cracks. All of this can be done nondestructively. No internal crack nor die surface delamination is allowed in this inspection.

External physical dimensions are measured per JEDEC JESD22 - B100. The measurements are compared to the currently active specification for the device in test. Failure can result in lot rejection, supplier disqualification, or correction to the specification.

Solderability is tested per MIL-STD-883, Method 2003. All leads are dipped on a sample size of three units, then 24 leads on the three devices are inspected. Type R Flux is used. Accept criteria is 95% coverage. For the Modules, type RMA Flux is used and acceptance criteria is 90% coverage.

Lead Integrity is tested to JEDEC JESD22 - B105. Twenty-four leads are tested on a sample size of six units. A 15° bend is used for Plastic DIP and SOIC.

Radiography (X-ray) is performed per MIL-STD-883, Method 2012. Top and side views of x-rays are recorded on film.

X-ray fluorescence is performed to verify plating thickness and composition.

External visual is performed per an internal DSC specification (27-03510-000) in order to verify the correct marking and external package integrity.

**Summary**

A summary of all stress tests used in the Reliability Monitor and the sample sizes used with each test are included with each report.