

RELIABILITY REPORT
FOR
DG412Fxxx
PLASTIC ENCAPSULATED DEVICES

April 17, 2003

MAXIM INTEGRATED PRODUCTS

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SUNNYVALE, CA 94086

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Conclusion

The DG412F successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The DG412F is a quad, single-pole/single-throw (SPST), fault-protected analog switch. It is pin compatible with the industry-standard nonprotected DG413. This new switch features fault-protected inputs and Rail-to-Rail™ signal-handling capability. All terminals are protected from overvoltage faults up to $\pm 36\text{V}$ with power on and up to $\pm 40\text{V}$ with power off. During a fault condition, the COM, NO, or NC terminal becomes an open circuit and only microamperes of leakage current flow from the source. On-resistance is 35Ω (max) and is matched between switches to 1.5Ω (max) at $+25^\circ\text{C}$.

The DG412F has four normally open switches. This CMOS switch operates with dual power supplies ranging from $\pm 4.5\text{V}$ to $\pm 20\text{V}$ or a single supply between $+9\text{V}$ and $+36\text{V}$. All digital inputs have $+0.8\text{V}$ and $+2.4\text{V}$ logic thresholds, ensuring both TTL and CMOS logic compatibility when using $\pm 15\text{V}$ or a single $+12\text{V}$ supply

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
(Voltages Referenced to GND)	
V+	-0.3V to +44V
V-	-44V to +0.3V
V+ to V-	-0.3V to +44V
IN_	(V- - 0.3V) to (V- + 40V)
NO_, NC_ to COM_ (Note 1)	-40V to +40V
COM_, NO_, NC_ Voltage with Power On (Note 1)	-36V to +36V
COM_, NO_, NC_ Voltage with Power Off (Note 1)	-40V to +40V
Continuous Current (any terminal_)	$\pm 30\text{mA}$
Peak Current COM_, NO_, NC_ (pulsed at 1ms, 10% duty cycle)	$\pm 100\text{mA}$
Operating Temperature Range	-40°C to $+85^\circ\text{C}$
Junction Temperature	$+150^\circ\text{C}$
Storage Temperature Range	-65°C to $+160^\circ\text{C}$
Lead Temperature (soldering, 10s)	$+300^\circ\text{C}$
Continuous Power Dissipation (TA= $+70^\circ\text{C}$)	
16-Pin DIP	842mW
16-Pin SO	696mW
16-Pin TSSOP	755mW
Derates above $+70^\circ\text{C}$	
16-Pin DIP	$10.53\text{mW}/^\circ\text{C}$
16-Pin SO	$8.7\text{mW}/^\circ\text{C}$
16-Pin TSSOP	$9.4\text{mW}/^\circ\text{C}$

Note 1: COM_, NO_, and NC_ pins are fault protected. Signals on COM_, NO_, and NC_ exceeding -36V to $+36\text{V}$ may damage the device during power-on conditions. When the power is off, the maximum range is -40V to $+40\text{V}$

II. Manufacturing Information

A. Description/Function:	Quad, Rail-to-Rail, Fault-Protected, SPST Analog Switches
B. Process:	S5HV (Medium voltage 5 micron silicon gate CMOS)
C. Number of Device Transistors:	251
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	February, 1994

III. Packaging Information

A. Package Type:	16-Lead SO	16-Lead DIP	16-Lead TSSOP
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1201-0289	# 05-1201-0287	# 05-1201-0288
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity Per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

IV. Die Information

A. Dimensions:	86 x 138 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 13.57 \times 10^{-9}$$

$$\lambda = 13.57 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5002) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AH88-1 die type has been found to have all pins able to withstand a transient pulse of <200, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit).

Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

DG412Fxxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	PDIP	77	0
			SO	77	0
			TSSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic package/process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

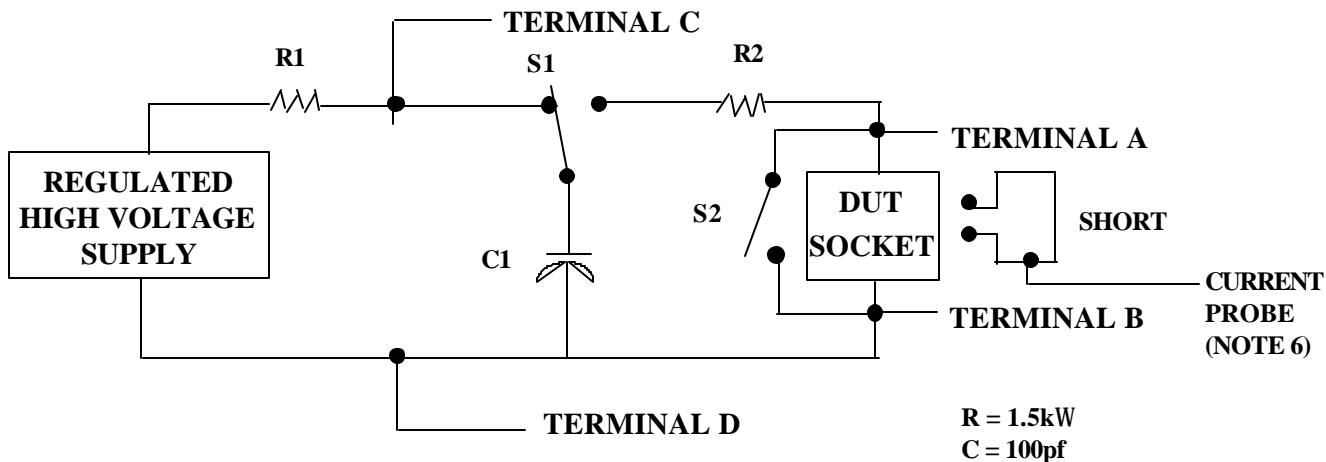
1/ Table II is restated in narrative form in 3.4 below.

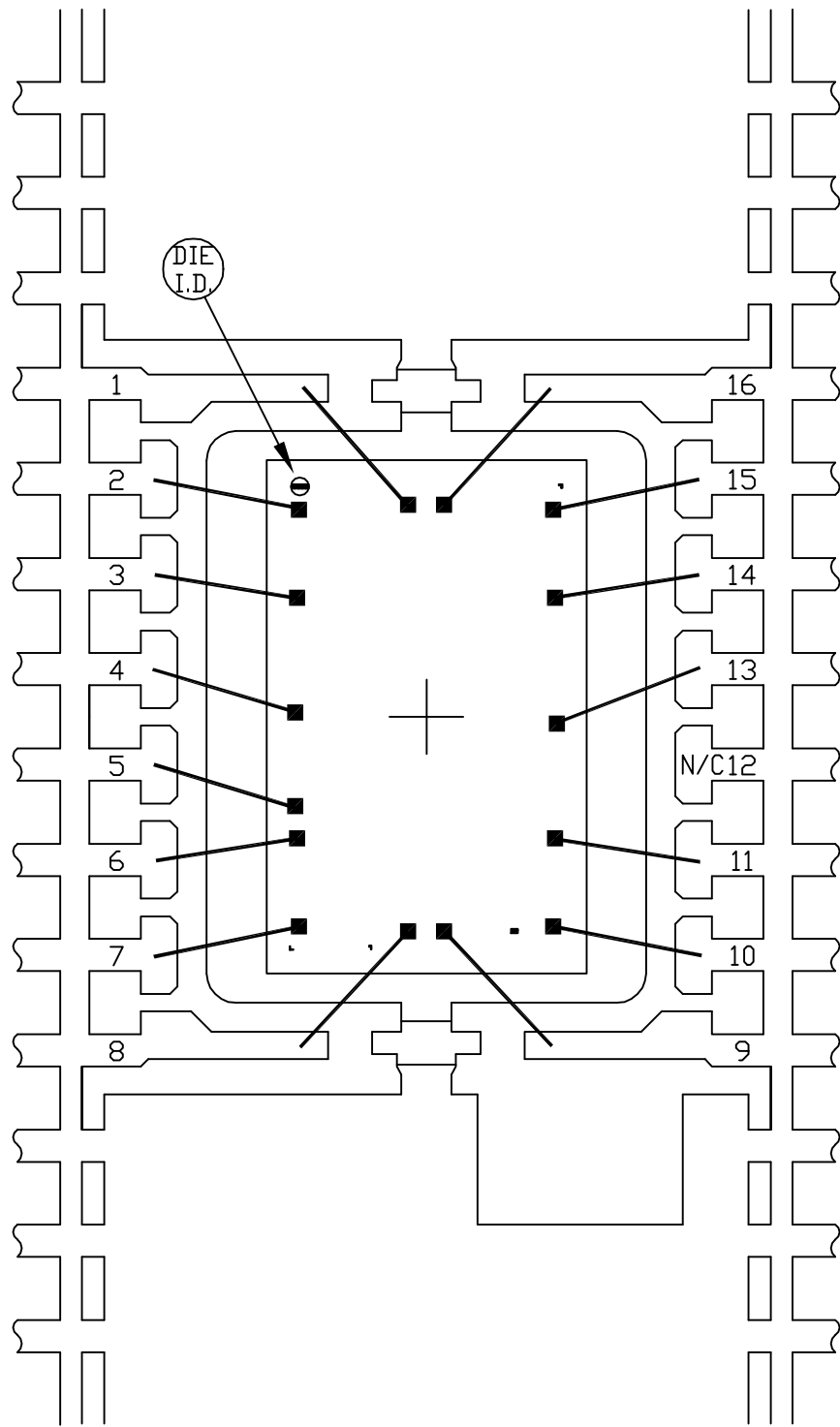
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

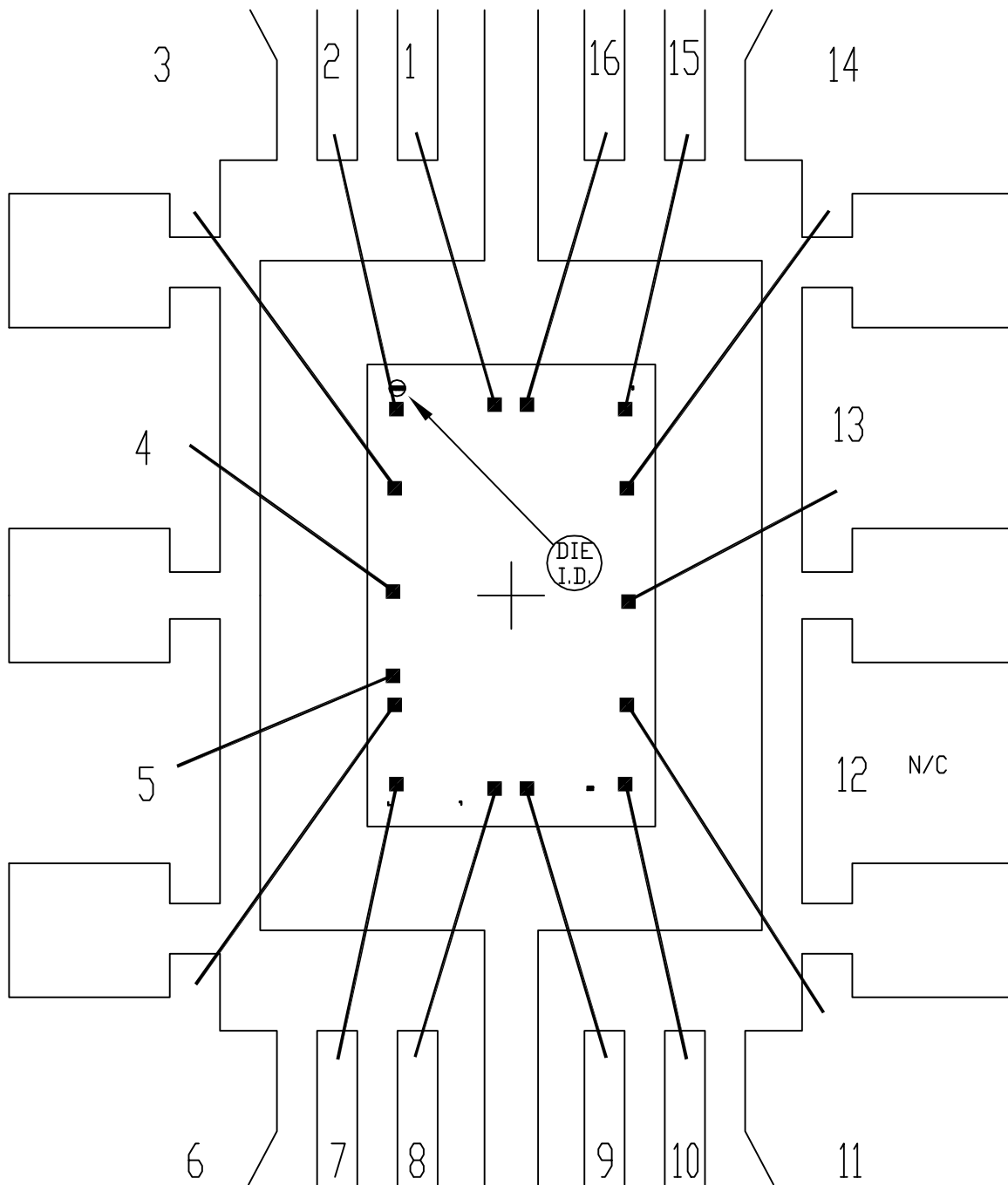
3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

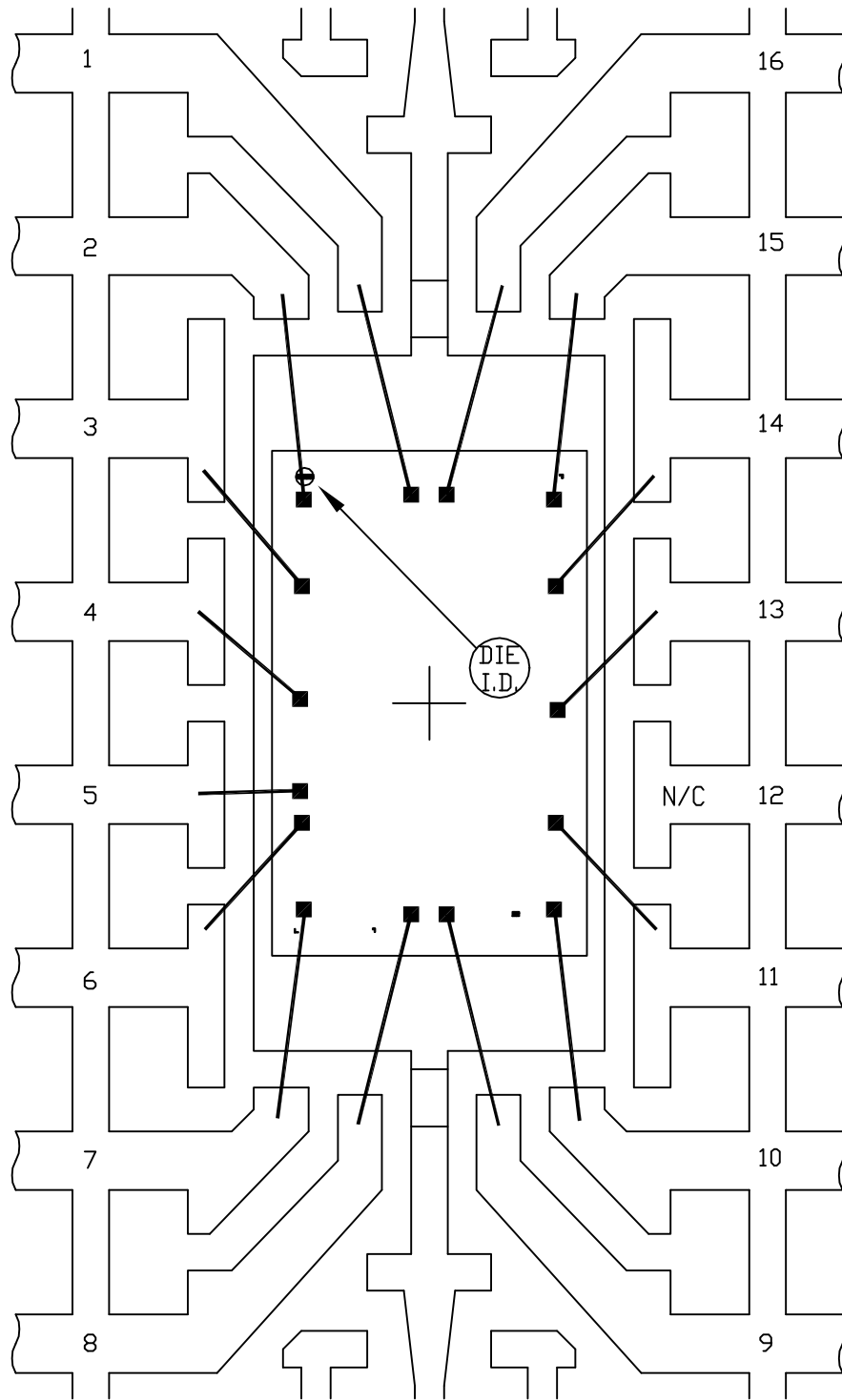




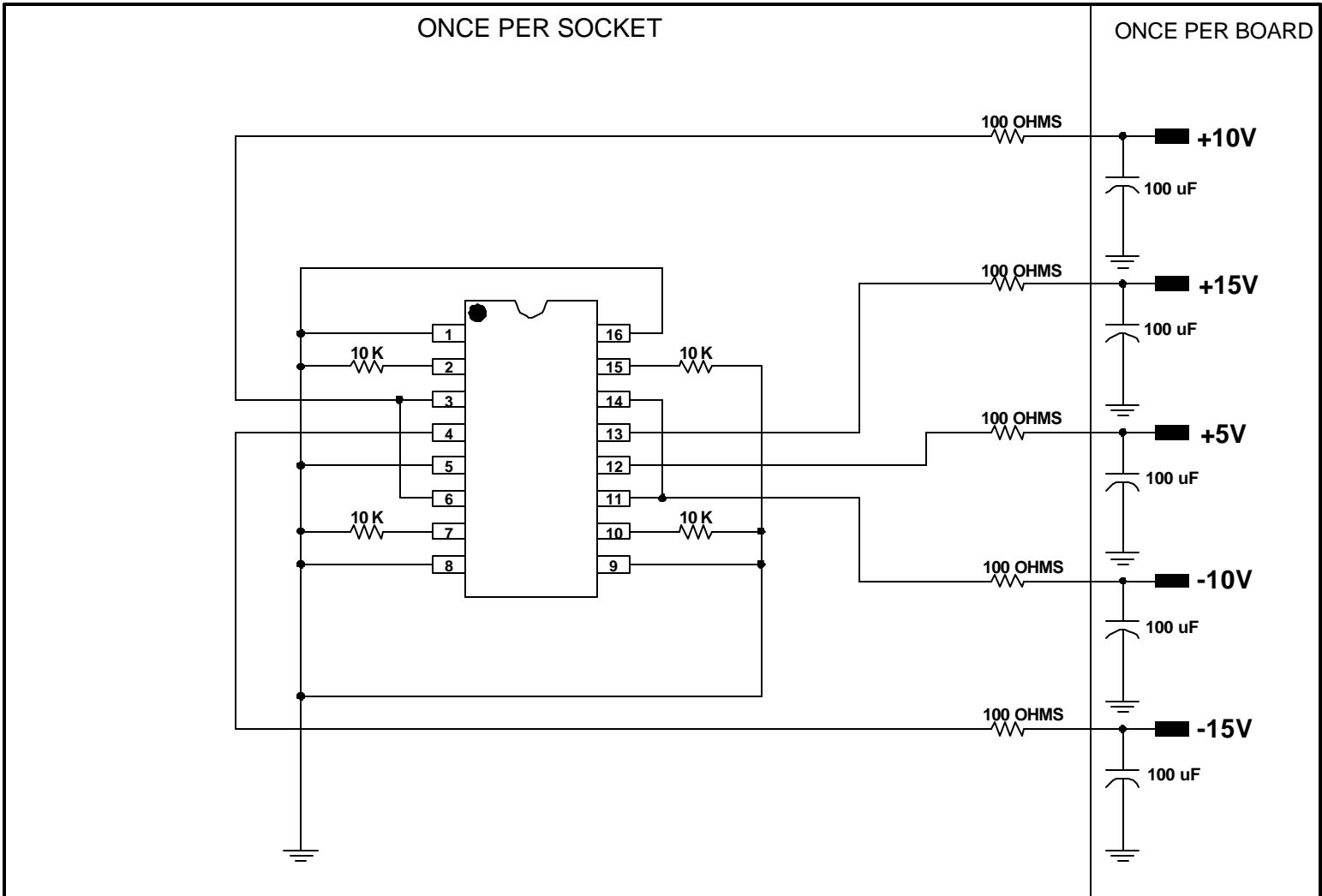
PKG. CODE: U16-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118X154	PKG. DESIGN			BOND DIAGRAM #: 05-1201-0288	REV: A



PKG. CODE: P16-3		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 150x200	PKG. DESIGN			BOND DIAGRAM #: 05-1201-0287	REV: A



PKG. CODE: S16-5		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 96X190	PKG. DESIGN			BOND DIAGRAM #: 05-1201-0289	REV: A



<p>DEVICES: MAX 327/332/352/353/362/365/313L/314L, DG202/212/309/412/413/445 PACKAGE: 16-(NARROW) SOIC DG412F/413F/313F/314F MAX. EXPECTED CURRENT= 10uA (ALL VOLTAGES)</p>	<p>DRAWN BY: TEK TAN NOTES: Max current from -10v is 2.5mA for MAX314/314L/353/DG413/413F/314F</p>
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