

RELIABILITY REPORT
FOR
MAX1510ETB+
PLASTIC ENCAPSULATED DEVICES

October 20, 2008

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Approved by
Ken Wendel
Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX1510ETB+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1510 DDR linear regulator sources and sinks up to 3A peak (typ) using internal n-channel MOSFETs. This linear regulator delivers an accurate 0.5V to 1.5V output from a low-voltage power input ($V_{IN} = 1.1V$ to 3.6V). The MAX1510 uses a separate 3.3V bias supply to power the control circuitry and drive the internal n-channel MOSFETs. The MAX1510 provides current and thermal limits to prevent damage to the linear regulator. Additionally, the MAX1510 generates a power-good (PGOOD) signal to indicate that the output is in regulation. During startup, PGOOD remains low until the output is in regulation for 2ms (typ). The internal soft-start limits the input surge current. The MAX1510 powers the active-DDR termination bus that requires a tracking input reference. The MAX1510 can also be used in low-power chipsets and graphics processor cores that require dynamically adjustable output voltages. The MAX1510 is available in a 10-pin 3mm x 3mm thin DFN package.

II. Manufacturing Information

A. Description/Function:	Low-Voltage DDR Linear Regulator
B. Process:	S4
C. Number of Device Transistors:	0
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Unisem, ISPL
F. Date of Initial Production:	April 24, 2004

III. Packaging Information

A. Package Type:	10-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-0813
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8.5°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8.5°C/W

IV. Die Information

A. Dimensions:	54 X 56 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.37 \times 10^{-9}$$

$$\lambda = 22.37 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at <http://www.maxim-ic.com/>. Current monitor data for the S4 Process results in a FIT Rate of 0.14 @ 25C and 2.42 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The PD46 die type has been found to have all pins able to withstand a HBM transient pulse of 2500V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of 250 mA.

Table 1
Reliability Evaluation Test Results

MAX1510ETB+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2) 85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2) Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data