

RELIABILITY REPORT  
FOR  
MAX19506ETM+  
PLASTIC ENCAPSULATED DEVICES

January 12, 2009

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
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## Conclusion

The MAX19506ETM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX19506 dual-channel, analog-to-digital converter (ADC) provides 8-bit resolution and a maximum sample rate of 100Msps.

The MAX19506 analog input accepts a wide 0.4V to 1.4V input common-mode voltage range, allowing DC-coupled inputs for a wide range of RF, IF, and baseband front-end components. The MAX19506 provides excellent dynamic performance from baseband to high input frequencies beyond 400MHz, making the device ideal for zero-intermediate frequency (ZIF) and high-intermediate frequency (IF) sampling applications. The typical signal-to-noise ratio (SNR) performance is 49.8dBFS and typical spurious-free dynamic range (SFDR) is 69dBc at  $f_{IN} = 70\text{MHz}$  and  $f_{CLK} = 100\text{MHz}$ .

The MAX19506 operates from a 1.8V supply. Additionally, an integrated, self-sensing voltage regulator allows operation from a 2.5V to 3.3V supply (AVDD). The digital output drivers operate on an independent supply voltage (OVDD) over the 1.8V to 3.5V range. The analog power consumption is only 57mW per channel at  $V_{AVDD} = 1.8\text{V}$ . In addition to low operating power, the MAX19506 consumes only 1mW in power-down mode and 17mW in standby mode.

Various adjustments and feature selections are available through programmable registers that are accessed through the 3-wire serial-port interface. Alternatively, the serial-port interface can be disabled, with the three pins available to select output mode, data format, and clock-divider mode. Data outputs are available through a dual parallel CMOS-compatible output data bus that can also be configured as a single multiplexed parallel CMOS bus.

The MAX19506 is available in a small 7mm x 7mm, 48-pin thin QFN package and is specified over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  extended temperature range.

Refer to the MAX19515, MAX19516, and MAX19517 data sheets for pin- and feature-compatible 10-bit, 65Msps, 100Msps, and 130Msps versions, respectively. Refer to the MAX19505 and MAX19507 data sheets for pin- and feature-compatible 8-bit, 65Msps and 130Msps versions, respectively.

## II. Manufacturing Information

A. Description/Function:	Dual-Channel, 8-Bit, 100Msps ADC
B. Process:	0.18um 1 Poly 6 Metal
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	ASAT China, UTL Thailand
F. Date of Initial Production:	10/16/2008

## III. Packaging Information

A. Package Type:	48-pin TQFN 7x7
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	36°C/W
K. Single Layer Theta Jc:	0.8°C/W
L. Multi Layer Theta Ja:	25°C/W
M. Multi Layer Theta Jc:	0.8°C/W

## IV. Die Information

A. Dimensions:	146 X 138 mils
B. Passivation:	Laser/TEOS Ox - Pass/Nit -PreLP+GenLP
C. Interconnect:	Al/Cu 0.5%
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO2
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- |                                   |   |
|-----------------------------------|---|
| A. Quality Assurance Contacts:    | Ken Wendel (Director, Reliability Engineering)<br>Bryan Preeshl (Managing Director of QA)       |
| B. Outgoing Inspection Level:     | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% For all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm  |
| D. Sampling Plan:                 | Mil-Std-105D  |

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.4 \times 10^{-9}$$

$$\lambda = 22.4 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at <http://www.maxim-ic.com/>. Current monitor data for the TSMC 0.18um Process results in a FIT Rate of 0.8 @ 25C and 13.1 @ 55C (0.8 eV, 60% UCL)

### B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

### C. E.S.D. and Latch-Up Testing

The CA24 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA, 1.5x VccMax V-Test.

**Table 1**  
Reliability Evaluation Test Results

**MAX19506ETM+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
<b>Moisture Testing</b> (Note 2) 85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b> (Note 2) Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data