

RELIABILITY REPORT  
FOR  
**MAX1968EUI**  
PLASTIC ENCAPSULATED DEVICES

October 29, 2002

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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## Conclusion

The MAX1968 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX1968 is a highly integrated and cost-effective, high-efficiency, switch-mode driver for Peltier thermoelectric cooler (TEC) modules. The device utilizes direct current control to eliminate current surges in the TEC. On-chip FETs minimize external components while providing high efficiency. A 500kHz/1MHz switching frequency and a unique ripple cancellation scheme reduce component size and noise.

The MAX1968 operates from a single supply and provides bipolar  $\pm 3A$  output by biasing the TEC between the outputs of two synchronous buck regulators. Bipolar operation allows for temperature control without "dead zones" or other nonlinearities at low load currents. This arrangement ensures that the control system does not hunt when the set point is very close to the natural operating point, requiring a small amount of heating or cooling. An analog control signal precisely sets the TEC current.

The MAX1968 is available in a low-profile 28-pin TSSOP-EP package and is specified over the  $-40^{\circ}C$  to  $+85^{\circ}C$  temperature range. The thermally-enhanced TSSOP-EP package with exposed metal pad minimizes operating junction temperature. An evaluation kit is available to speed designs.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
VDD to GND	-0.3V to +6V
SHDN, MAXV, MAXIP, MAXIN, CTLI, FREQ to GND	-0.3V to +6V
COMP, OS1, OS2, CS, REF, ITEC to GND	-0.3V to (VDD + 0.3V)
PVDD1, PVDD2 to GND	-0.3V to (VDD + 0.3V)
PVDD1, PVDD2 to VDD	-0.3V to +0.3V
PGND1, PGND2 to GND	-0.3V to +0.3V
COMP, REF, ITEC Short to GND	Indefinite
Peak LX Current (MAX1968) (Note 1)	$\pm 4.5A$
Peak LX Current (MAX1969) (Note 1)	+9A
Operating Temperature Range	$-40^{\circ}C$ to $+85^{\circ}C$
Maximum Junction Temperature	$+150^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $+150^{\circ}C$
Lead Temperature (soldering 10s)	$+300^{\circ}C$
Continuous Power Dissipation (TA = $+70^{\circ}C$ )	
28-Pin TSSOP-EP	1.9W
Derates above $+70^{\circ}C$	
28-Pin TSSOP-EP	23.8mW/ $^{\circ}C$

**Note 1:** LX has internal clamp diodes to PGND and PVDD\_. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

## II. Manufacturing Information

A. Description/Function:	Power Drivers for Peltier TEC Modules
B. Process:	S8 - Standard 8 micron silicon gate CMOS
C. Number of Device Transistors:	2959
D. Fabrication Location:	California, USA
E. Assembly Location:	Philippines
F. Date of Initial Production:	April, 2002

## III. Packaging Information

A. Package Type:	<b>28-Lead TSSOP</b>
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (2.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-3501-0019
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

## IV. Die Information

A. Dimensions:	108 X 207 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	TiW/ AlCu/ TiWN
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

▲  
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 24.13 \times 10^{-9} \quad \lambda = 24.13 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-5865) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**) located on the Maxim website at <http://www.maxim-ic.com>.

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The PM29-4 die type has been found to have all pins able to withstand a transient pulse of  $\pm 200\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 50\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX1968EUI**

<b>TEST ITEM</b>	<b>TEST CONDITION</b>	<b>FAILURE IDENTIFICATION</b>	<b>SAMPLE SIZE</b>	<b>NUMBER OF FAILURES</b>
<b>Static Life Test</b> (Note 1)				
	Ta = 135°C biased Time = 192 hrs.	DC Parameters & functionality	45	0
<b>Moisture Testing</b> (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b> (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic process/package data

## Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

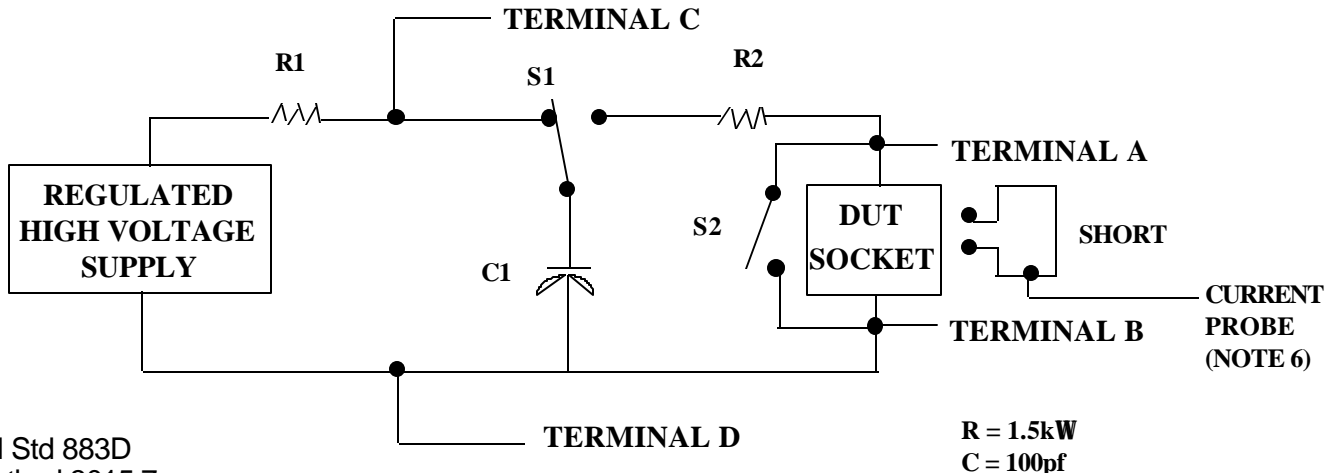
2/ No connects are not to be tested.

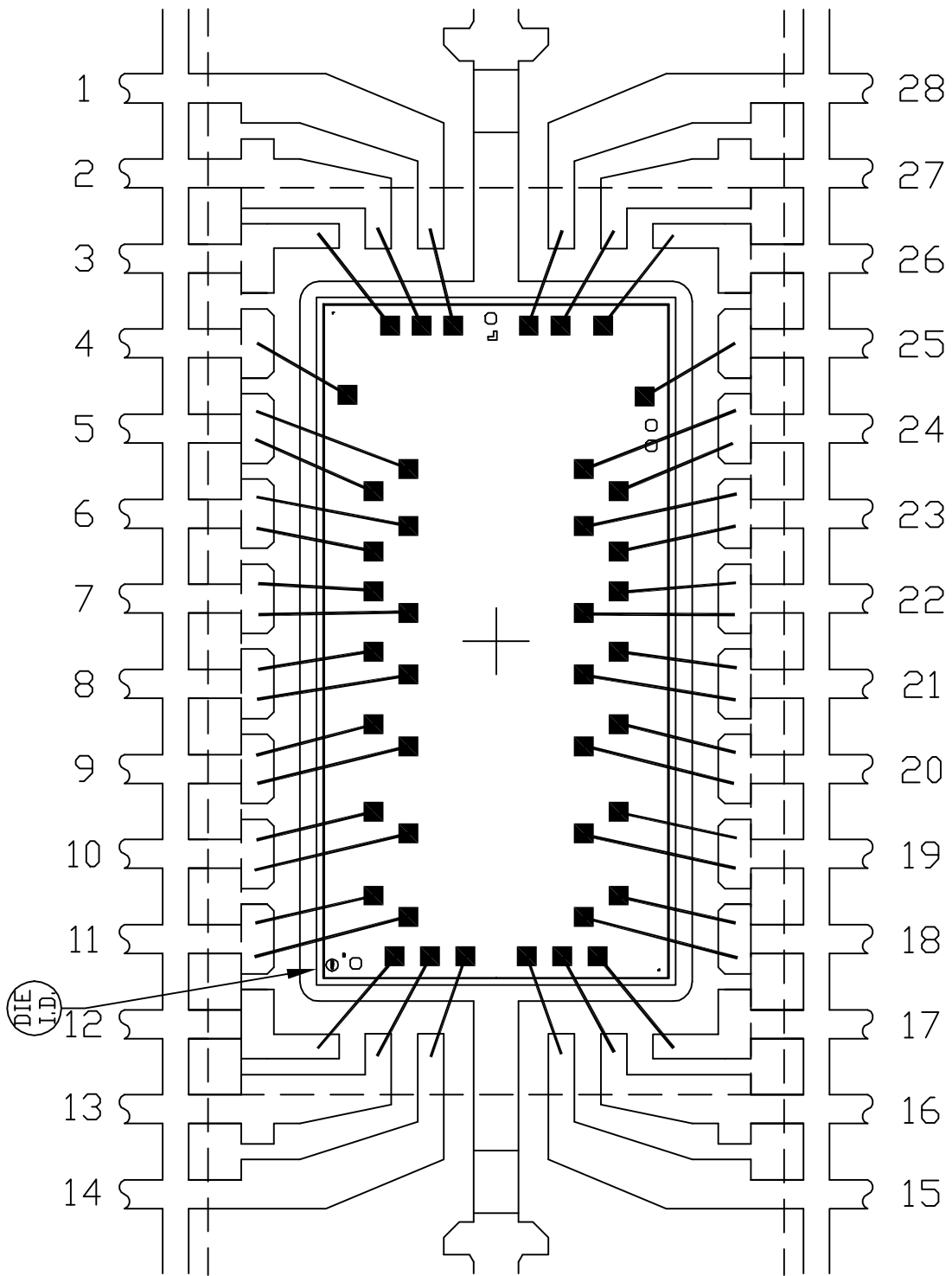
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

### 3.4 Pin combinations to be tested.

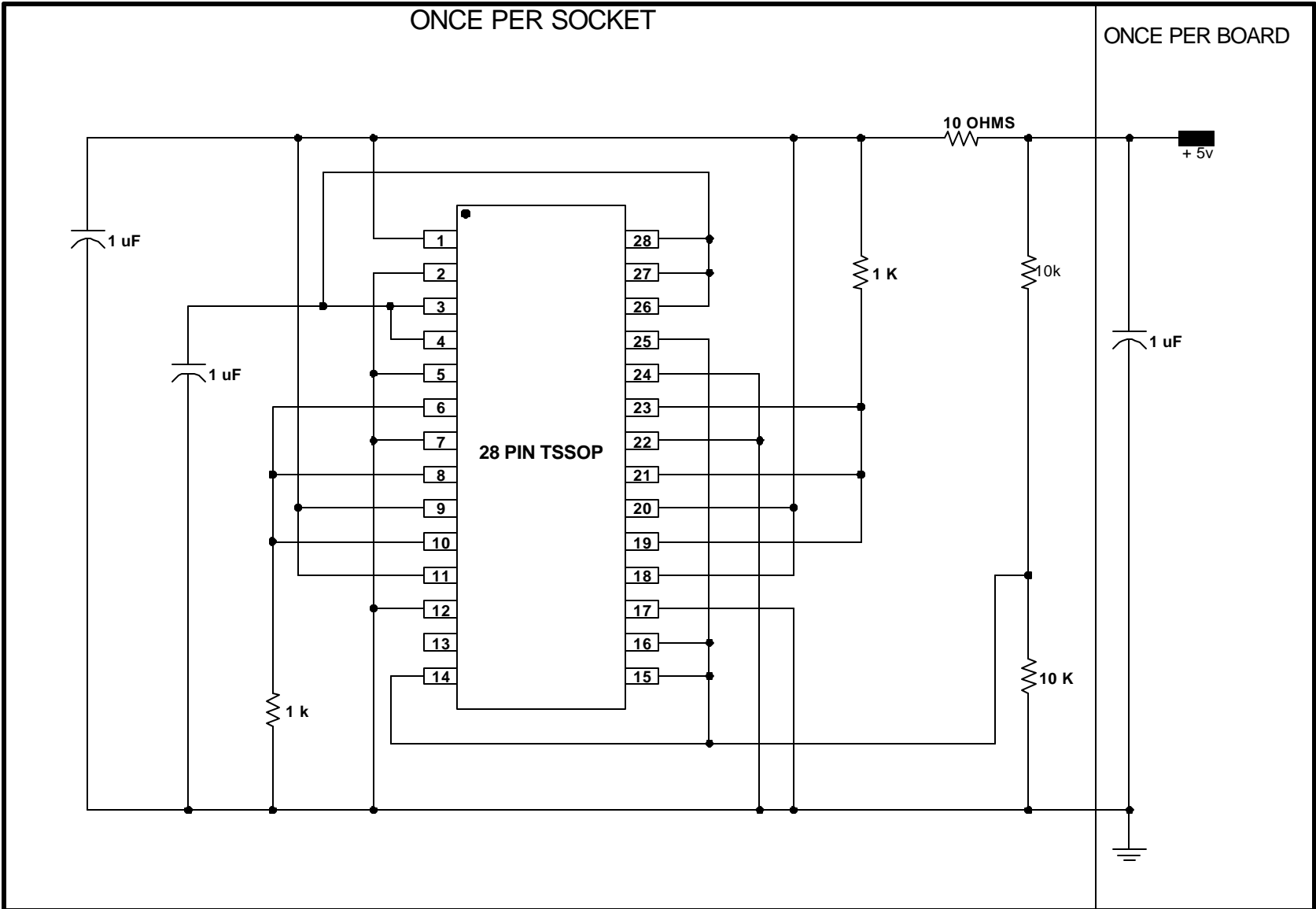
- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





EXPOSED PAD PKG.

PKG. CODE: U28E-4		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118x217	PKG. DESIGN			BOND DIAGRAM #: 05-3501-0019	REV: A



DEVICES: MAX 1968/1969

DRAWN BY: TEK TAN

MAX. EXPECTED CURRENT = 3 mA

NOTES: