

RELIABILITY REPORT
FOR
MAX333ACxx
PLASTIC ENCAPSULATED DEVICES

February 7, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX333A successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX333A is a precision, quad, single-pole double-throw (SPDT) analog switch. The four independent switches operate with bipolar supplies ranging from $\pm 4.5\text{V}$ to $\pm 20\text{V}$, or with a single-ended supply between $+10\text{V}$ and $+30\text{V}$. The MAX333A offers low on resistance (less than 35Ω), guaranteed to match within 2Ω between channels and to remain flat over the analog signal range ($\Delta 3\Omega$ max). It also offers break-before-make switching (10ns typical), with turn-off times less than 145ns and turn-on times less than 175ns. The MAX333A is ideal for portable operation since quiescent current runs less than $50\mu\text{A}$ with all inputs high or low.

This monolithic, quad switch is fabricated with Maxim's new improved silicon-gate process. Design improvements guarantee extremely low charge injection (10pC), and low power consumption (3.75mW).

Logic inputs are TTL and CMOS compatible and guaranteed over a $+0.8\text{V}$ to $+2.4\text{V}$ range – regardless of supply voltage. Logic inputs and switched analog signals can range anywhere between the supply voltages without damage.

B. Absolute Maximum Ratings

| <u>Item</u> | <u>Rating</u> |
|--|-----------------|
| V+ to V- | 44V |
| V _{IN} , V _{COM} , V _{NO} , V _{NC} (V _{NO} - V _{NC}) | V- to V+ |
| V+ to Ground | 32V |
| V- to Ground | 30V |
| Current, Any Terminal Except V _{COM} , V _{NO} , V _{NC} | -30V |
| Continuous Current, V _{COM} , V _{NO} , V _{NC} | 30mA |
| Peak Current, V _{COM} , V _{NO} , V _{NC} (Pulsed at 1ms, 10% duty cycle max) | 20mA |
| Storage Temp. | 70mA |
| Lead Temp. (10 sec.) | -65°C to +150°C |
| Continuous Power Dissipation (TA = +70°C) | +300°C |
| 20-Pin PDIP | 889mW |
| 20-Pin SO | 800mW |
| 20-Pin TSSOP | 559mW |
| Derates above +70°C | |
| 20-Pin PDIP | 11.11mW/°C |
| 20-Pin SO | 10.0mW/°C |
| 20-Pin TSSOP | 8.00mW/°C |

Note 1: Device mounted with all leads soldered to PC board.

II. Manufacturing Information

| | |
|----------------------------------|--|
| A. Description/Function: | Precision, Quad, SPDT, CMOS Analog Switch |
| B. Process: | S5 (SG5) - Standard 5 micron silicon gate CMOS |
| C. Number of Device Transistors: | 145 |
| D. Fabrication Location: | Oregon, USA |
| E. Assembly Location: | Philippines, Malaysia or Thailand |
| F. Date of Initial Production: | April, 1991 |

III. Packaging Information

| A. Package Type: | 20-Lead WSO | 16-Lead PDIP | 20-Lead TSSOP |
|---|--------------------------|--------------------------|--------------------------|
| B. Lead Frame: | Copper | Copper | Copper |
| C. Lead Finish: | Solder Plate | Solder Plate | Solder Plate |
| D. Die Attach: | Silver-filled Epoxy | Silver-filled Epoxy | Silver-filled Epoxy |
| E. Bondwire: | Gold (1.3 mil dia.) | Gold (1.3 mil dia.) | Gold (1.0 mil dia.) |
| F. Mold Material: | Epoxy with silica filler | Epoxy with silica filler | Epoxy with silica filler |
| G. Assembly Diagram: | # 05-0301-0614 | # 05-0301-0613 | # 05-0301-0869 |
| H. Flammability Rating: | Class UL94-V0 | Class UL94-V0 | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1 | Level 1 | Level 1 |

IV. Die Information

| | |
|----------------------------|---|
| A. Dimensions: | 101 x 139 mils |
| B. Passivation: | Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Si (Si = 1%) |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 5 microns (as drawn) |
| F. Minimum Metal Spacing: | 5 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | SiO ₂ |
| I. Die Separation Method: | Wafer Saw |

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{4.04}{192 \times 4389 \times 240 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 9.99 \times 10^{-9} \quad \lambda = 9.99 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-1742) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AG63 die type has been found to have all pins able to withstand a transient pulse of $\pm 1000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX333ACxx

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|-----------------------------------|---|----------------------------------|---------|-------------|--------------------|
| Static Life Test (Note 1) | | | | | |
| | Ta = 135°C Biased Time = 192 hrs. | DC Parameters & functionality | | 240 | 1 |
| Moisture Testing (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs. | DC Parameters & functionality | NSO | 77 | 0 |
| | | | PDIP | 77 | 0 |
| | | | TSSOP | 77 | 0 |
| 85/85 | Ta = 85°C RH = 85% Biased Time = 1000hrs. | DC Parameters & functionality | | 77 | 0 |
| Mechanical Stress (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C 1000 Cycles Method 1010 | DC Parameters & functionality | | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|----|---|---|
| 1. | All pins except V_{PS1} <u>3/</u> | All V_{PS1} pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.

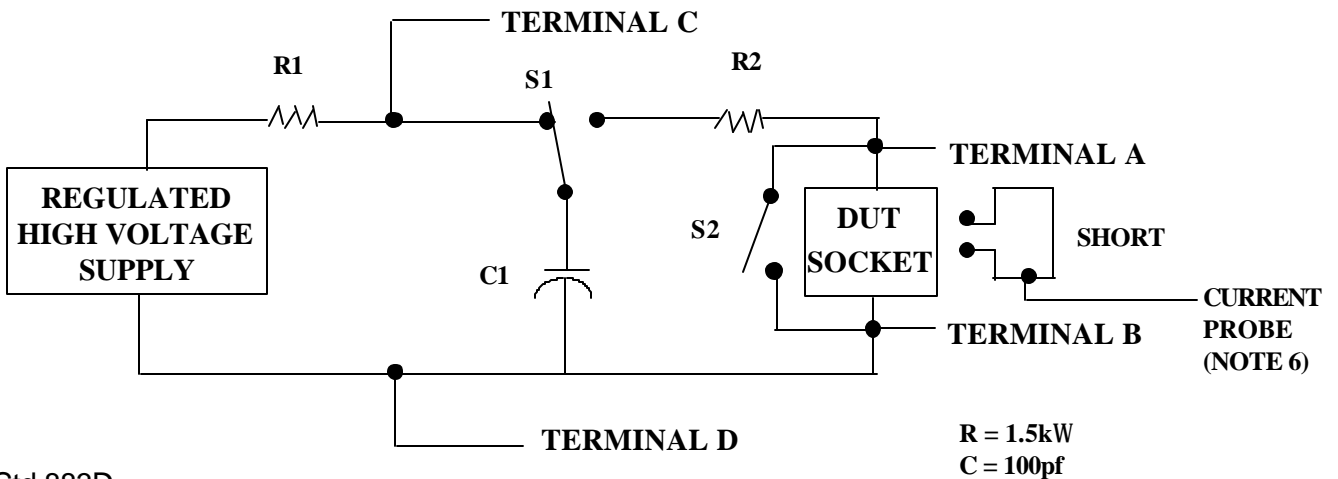
2/ No connects are not to be tested.

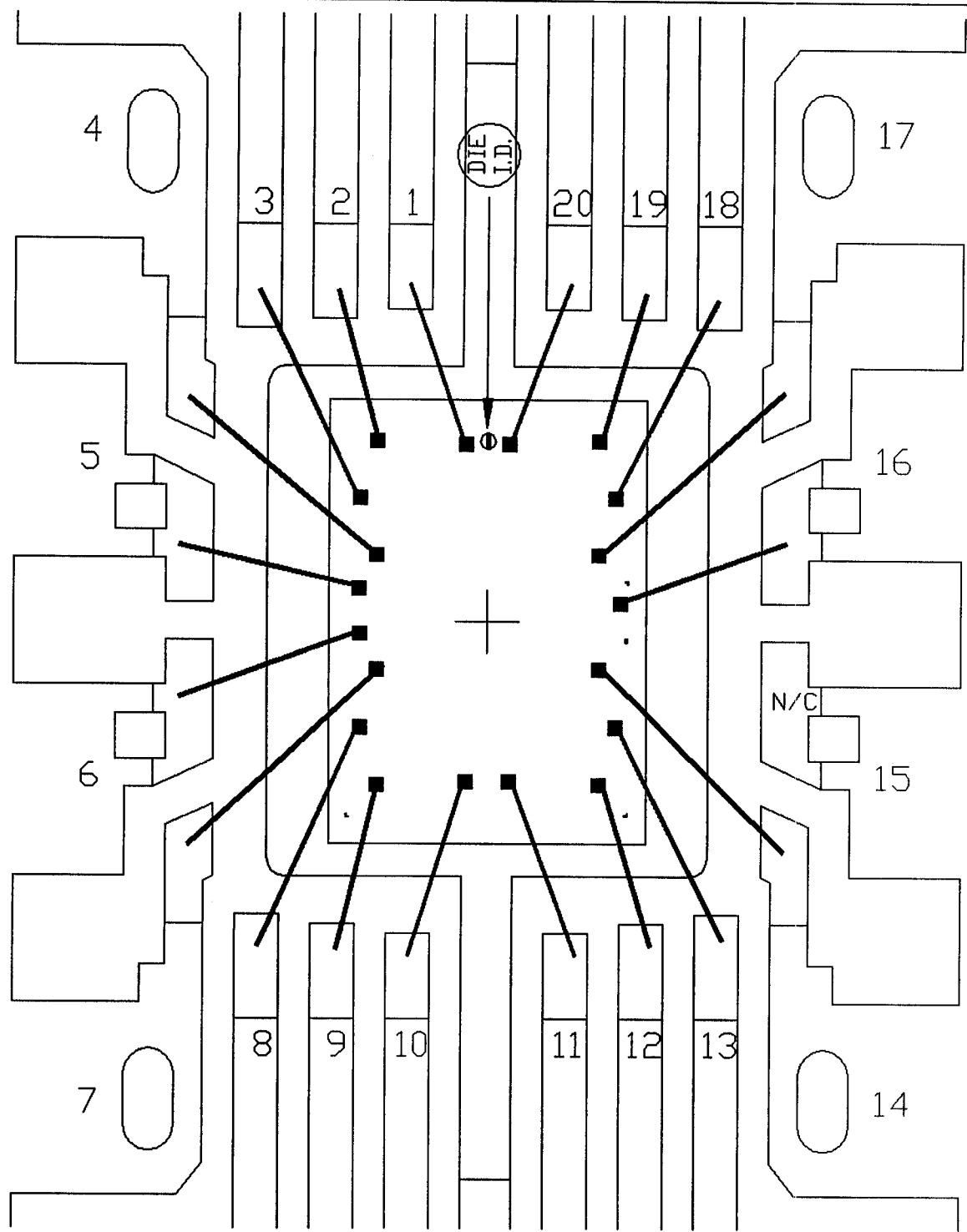
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: P20-5

CAV./PAD SIZE:
140X160

PKG.
DESIGN

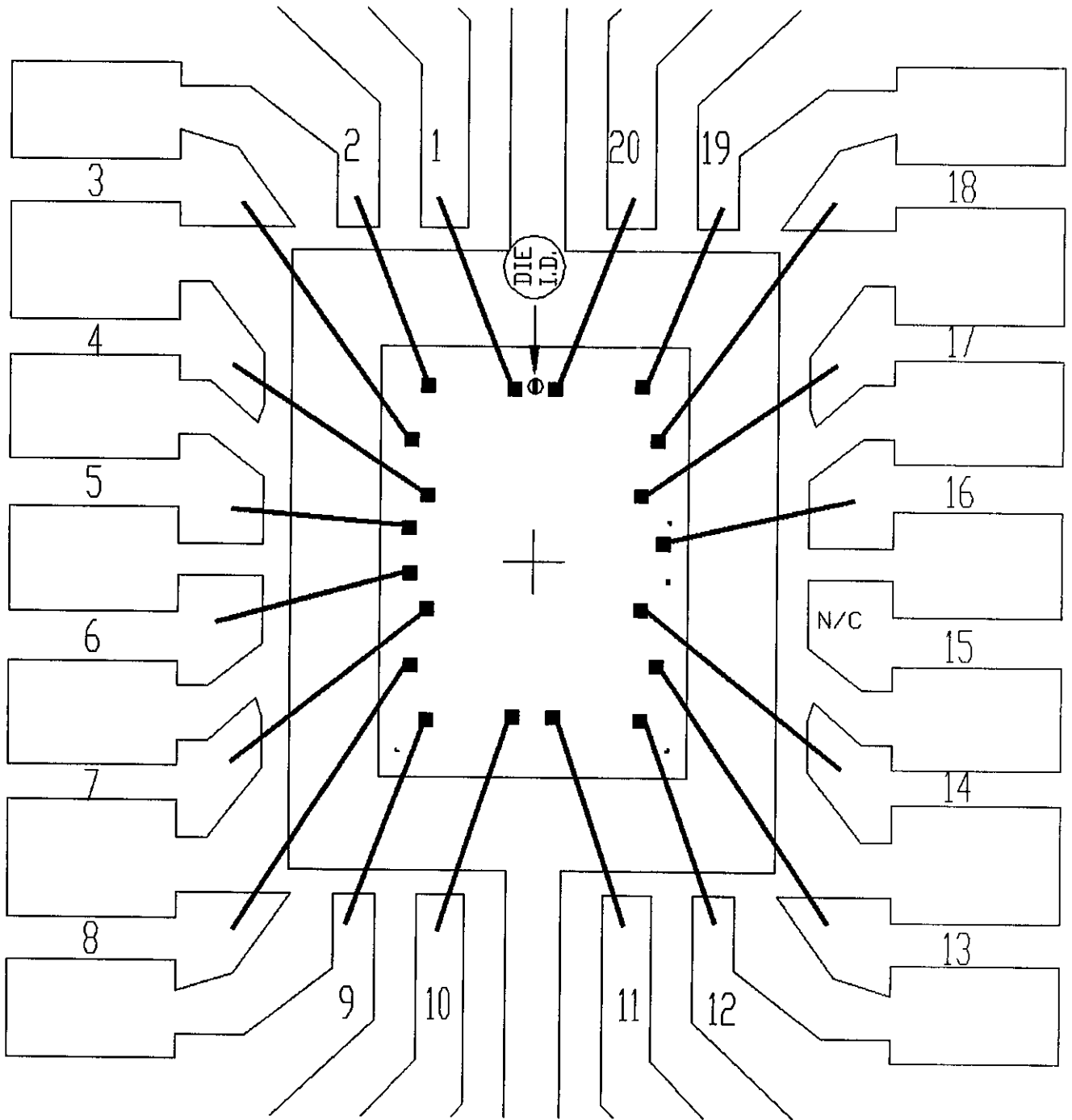
APPROVALS

DATE

MAXIM

BUILDSHEET NUMBER:
05-0301-0613

REV:
B

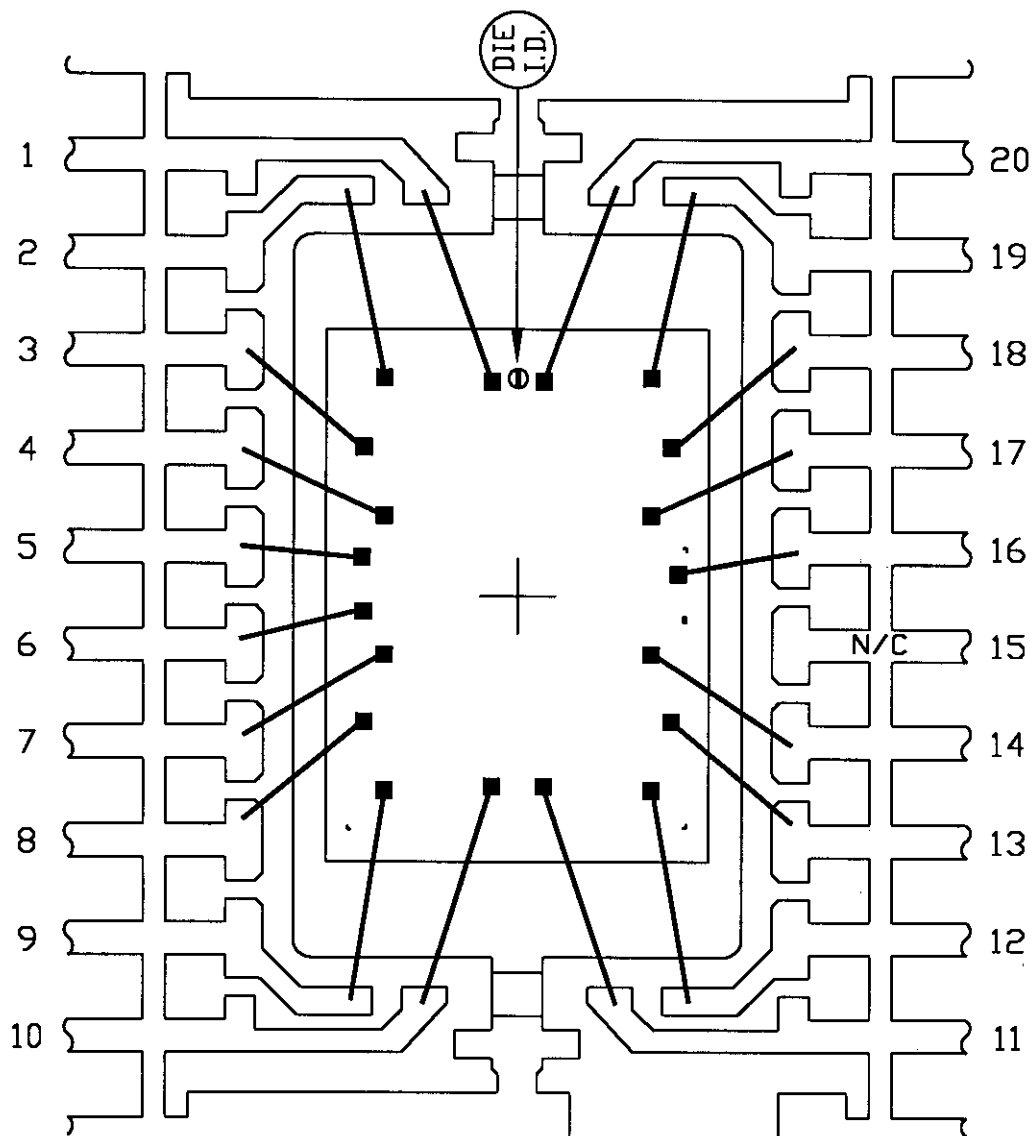


| | |
|--------------------------|-------------|
| PKG.CODE: W20-3 | |
| CAV./PAD SIZE: 160 X 200 | PKG. DESIGN |

APPROVALS

DATE

| | |
|---------------------------------|---------|
| MAXIM | |
| BUILDSHEET NUMBER: 05-0301-0614 | REV.: B |



PKG.CODE: U20-2

CAV./PAD SIZE:
118X189

APPROVALS

DATE

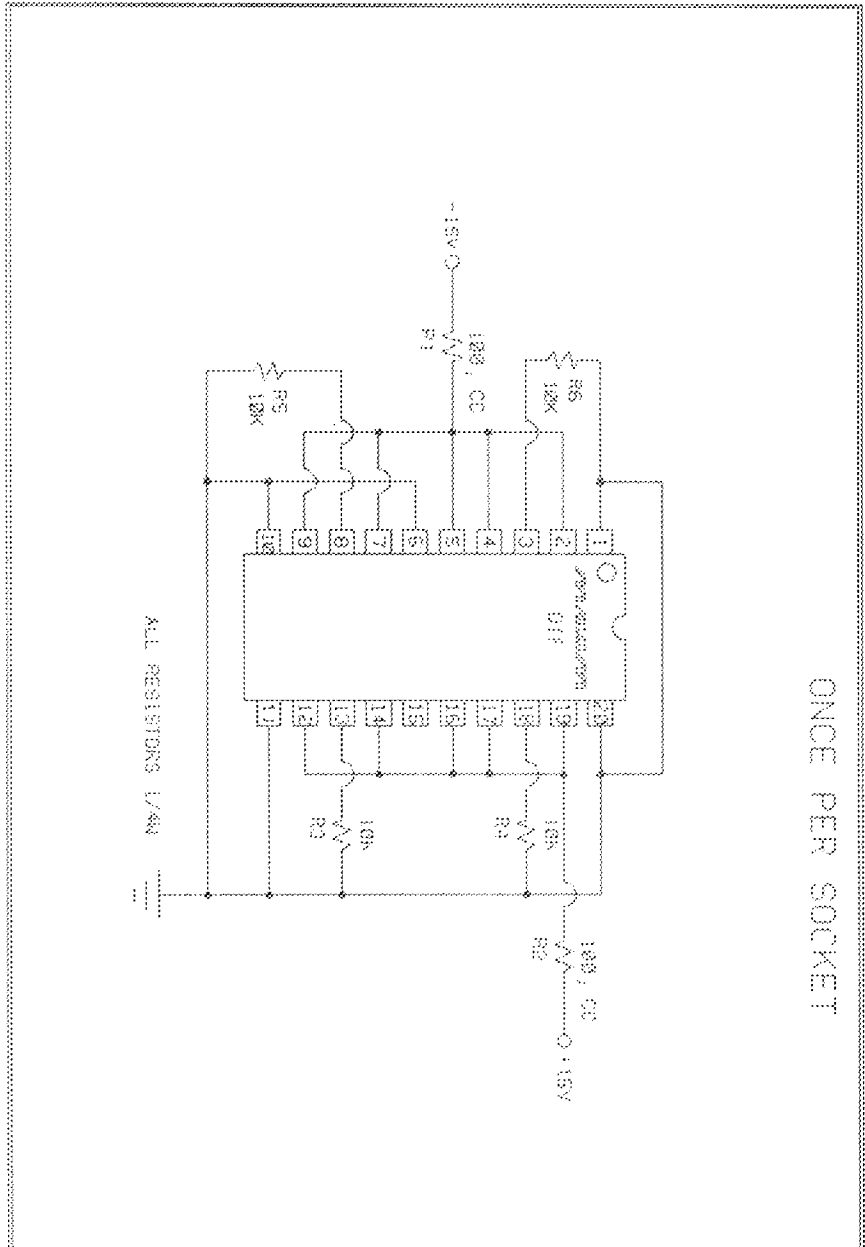
MAXIM

BUILDSHEET NUMBER:
05-0301-0869

REV.:
A

PKG.
DESIGN

ONCE PER SOCKET

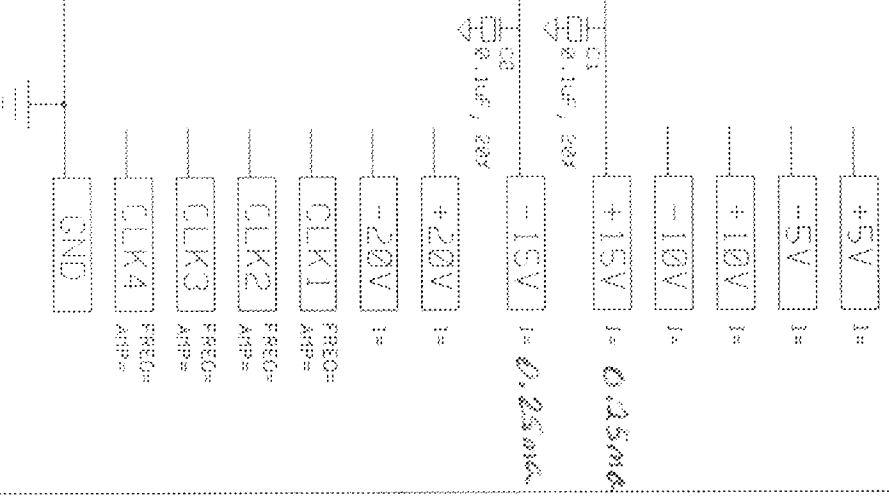


STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1046.
 BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 100 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 158C CONTINUOUS
4. APPROVED FOR (X) COMMERCIAL (X) MR/983

ONCE PER BOARD



| | | |
|--|---|---|
| <p>1. TEMPERATURE: 125C OR EQUIVALENT</p> <p>2. TIME: 100 HOURS MIN. OR EQUIVALENT</p> <p>3. ALL COMPONENTS AND MATERIAL MUST STAND 158C CONTINUOUS</p> <p>4. APPROVED FOR (X) COMMERCIAL (X) MR/983</p> | <p>SPEC. NO. 06-1742 REV. A</p> <p>DATE: 6/25/92</p> <p>DRAWN BY: N.K. NGUYEN</p> | <p>MAXIM BURN-IN SCHEMATIC</p> <p>DEVICE TYPE: MAX333</p> |
|--|---|---|