

RELIABILITY REPORT  
FOR  
**MAX3378EEUD**  
PLASTIC ENCAPSULATED DEVICES

March 6, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Reviewed by



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## Conclusion

The MAX3378E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

## Table of Contents

I. ....Device Description	V. ....Quality Assurance Information
II. ....Manufacturing Information	VI. ....Reliability Evaluation
III. ....Packaging Information	
IV. ....Die Information	.....Attachments

### I. Device Description

The MAX3378E  $\pm 15\text{kV}$  ESD-protected level translator provides the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages,  $V_{CC}$  and  $V_L$ , set the logic levels on either side of the device. A low-voltage logic signal present on the  $V_L$  side of the device appears as a high-voltage logic signal on the  $V_{CC}$  side of the device, and vice-versa. The MAX3378E bidirectional level translator utilizes a transmission-gate-based design (Figure 2) to allow data translation in either direction ( $V_L \Leftrightarrow V_{CC}$ ) on any single data line. The MAX3378E accept  $V_L$  from +1.2V to +5.5V and  $V_{CC}$  from +1.65V to +5.5V, making it ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems.

The MAX3378E features a three-state output mode that reduces supply current to less than  $1\mu\text{A}$ , thermal short-circuit protection, and  $\pm 15\text{kV}$  ESD protection on the  $V_{CC}$  side for greater protection in applications that route signals externally. The MAX3378E operates at a guaranteed data rate of 8Mbps over the entire specified operating voltage range. Within specific voltage domains, higher data rates are possible. (See *Timing Characteristics*.)

The MAX3378E is a quad level shifters available in 3 x 4 UCSP and 14-pin TSSOP packages.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
All Voltages Referenced to GND	
VCC	-0.3V to +6V
I/O VCC <sub>1</sub>	-0.3V to (VCC + 0.3V)
I/O VL <sub>1</sub>	-0.3V to (VL + 0.3V)
THREE-STATE	-0.3V to (VL + 0.3V)
Short-Circuit Duration I/O VL, I/O VCC to GND	Continuous
Short-Circuit Duration I/O VL or I/O VCC to GND Driven from 40mA Source	Continuous
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
14-Pin TSSOP	727mW
Derates above +70°C	
14-Pin TSSOP	9.1mW/°C

## II. Manufacturing Information

- A. Description/Function:  $\pm 15\text{kV}$  ESD-Protected,  $1\mu\text{A}$ , 16Mbps, Dual/Quad Low-Voltage Level Translators
- B. Process: S8
- C. Number of Device Transistors: 295
- D. Fabrication Location: Oregon, USA
- E. Assembly Location: Philippines or Thailand
- F. Date of Initial Production: April, 2002

## III. Packaging Information

- A. Package Type: **14-Lead TSSOP**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate
- D. Die Attach: Silver-filled Epoxy
- E. Bondwire: Gold (1.0 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: Buildsheet # 05-2601-0074
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

## IV. Die Information

- A. Dimensions: 80 x 61 mils
- B. Passivation:  $\text{Si}_3\text{N}_4/\text{SiO}_2$  (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Copper/Silicon
- D. Backside Metallization: None
- E. Minimum Metal Width: .8 microns (as drawn)
- F. Minimum Metal Spacing: .8 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric:  $\text{SiO}_2$
- I. Die Separation Method: Wafer Saw

## V. Quality Assurance Information

### A. Quality Assurance Contacts:

Jim Pedicord (Reliability Lab Manager)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 24.13 \times 10^{-9} \quad \lambda = 24.13 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5728) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The RT40-4 die type has been found to have all pins able to withstand a transient pulse of 1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX3378EEUD**

<b>TEST ITEM</b>	<b>TEST CONDITION</b>	<b>FAILURE IDENTIFICATION</b>	<b>SAMPLE SIZE</b>	<b>NUMBER OF FAILURES</b>
<b>Static Life Test</b> (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	45	0
<b>Moisture Testing</b> (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
<b>Mechanical Stress</b> (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

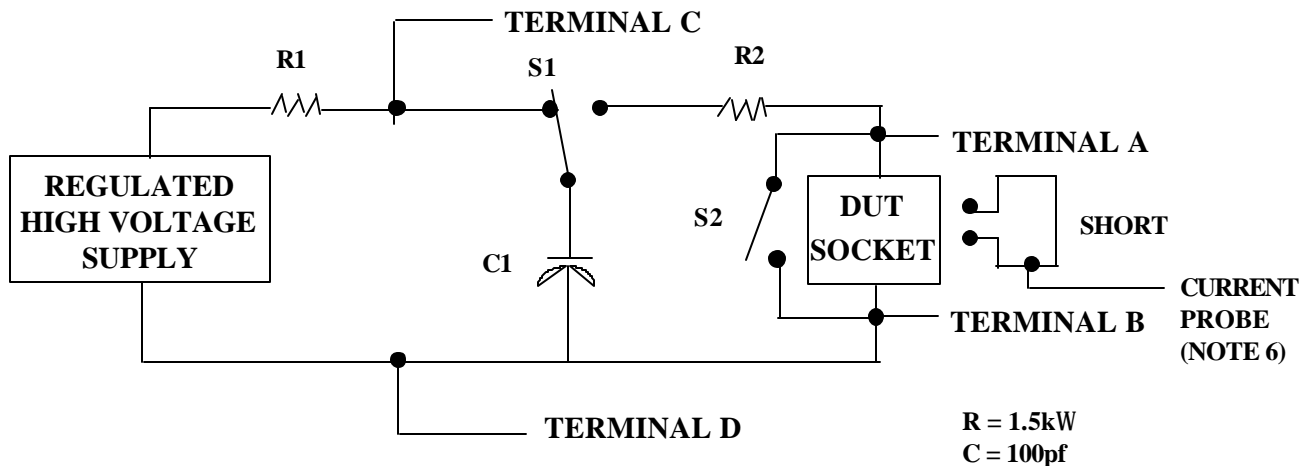
1/ Table II is restated in narrative form in 3.4 below.

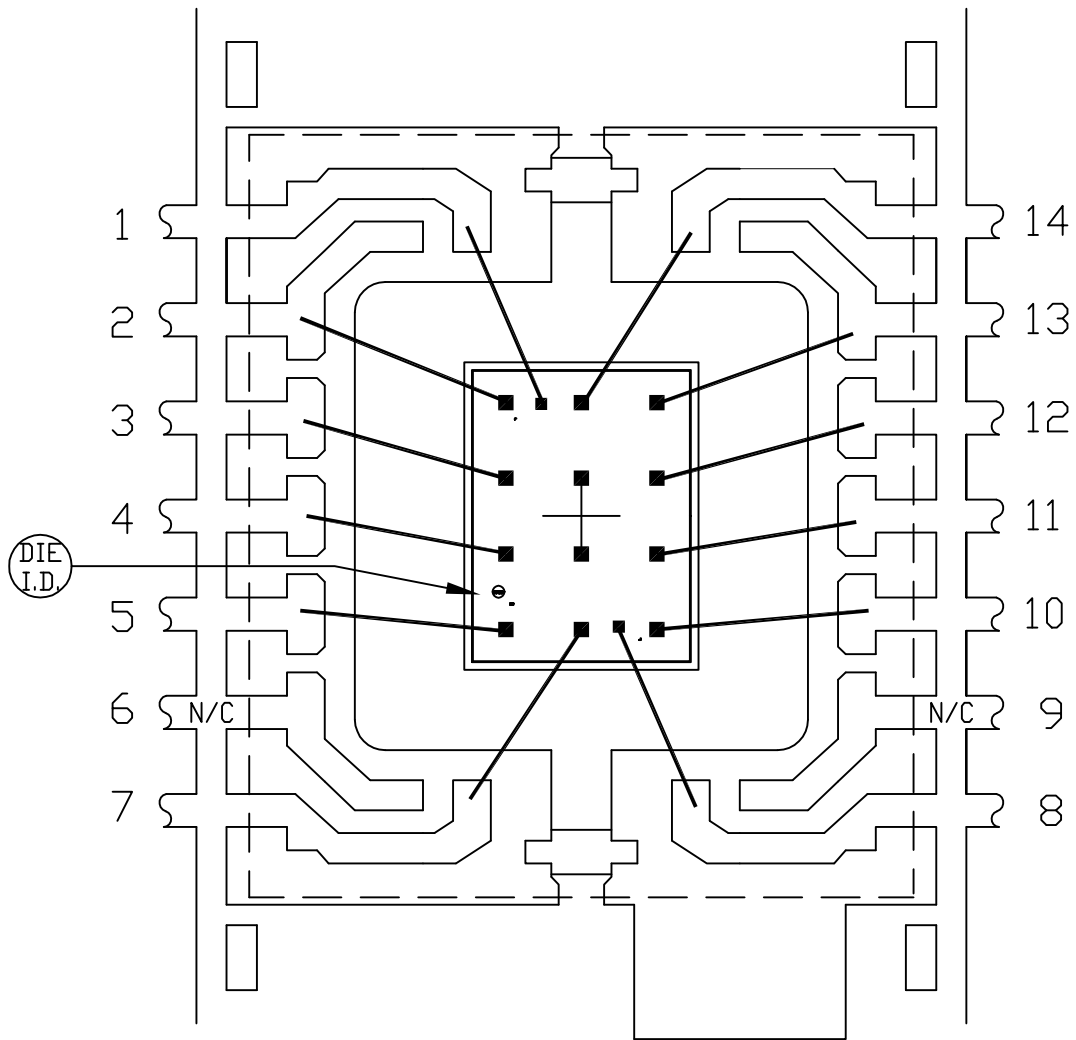
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground (e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



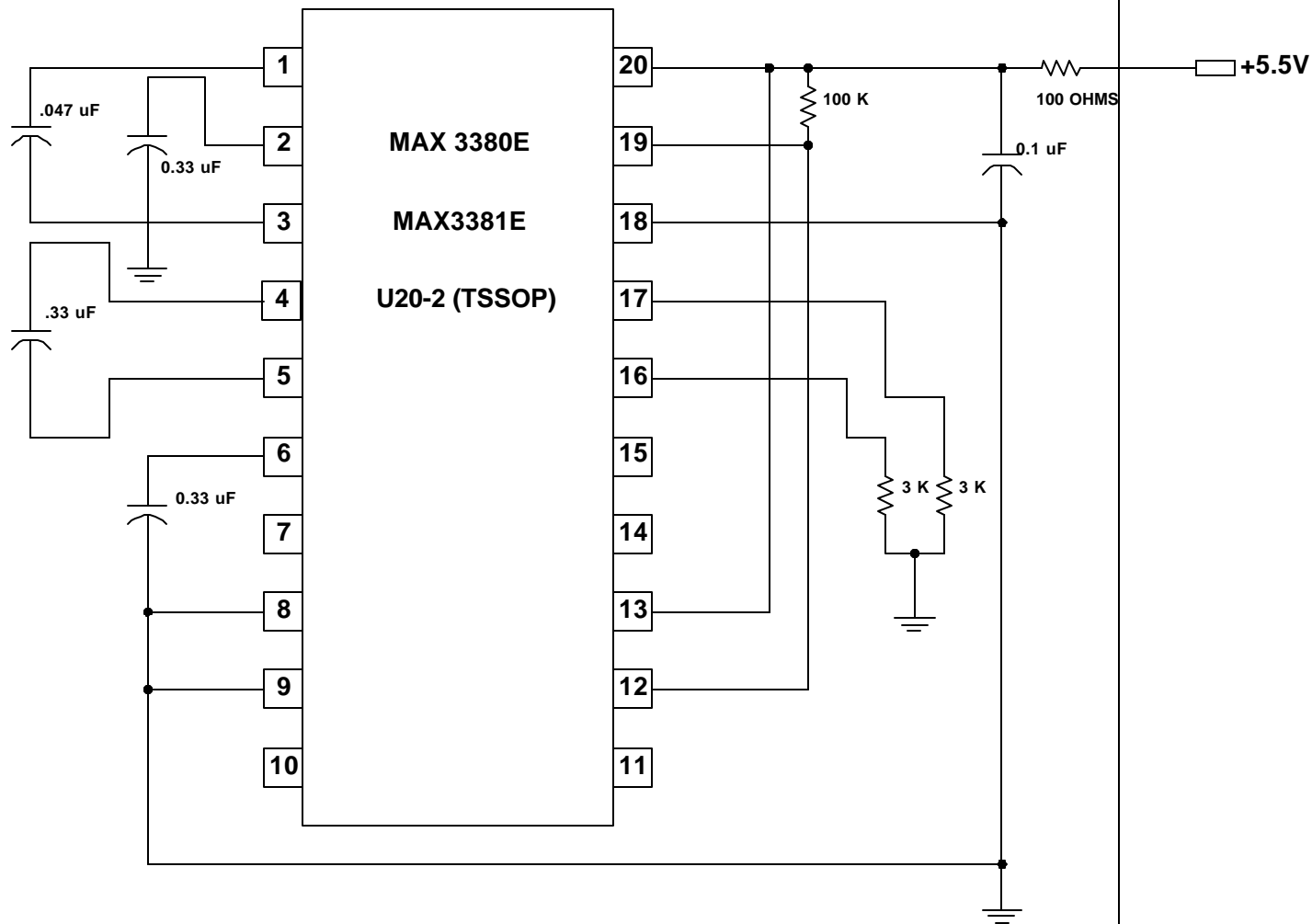


DIE  
I.D.

PKG. CODE: U14-1		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 118x122	PKG. DESIGN			BOND DIAGRAM #: 05-2601-0074	REV: A

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 3380E/1E

DRAWN BY: HAK TAN

MAX. EXPECTED CURRENT = 20mA

NOTES: