

RELIABILITY REPORT
FOR
MAX3670ETJ+
PLASTIC ENCAPSULATED DEVICES

August 7, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

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| Approved by |
| Ken Wendel |
| Quality Assurance |
| Director, Reliability Engineering |

Conclusion

The MAX3670ETJ+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3670 is a low-jitter 155MHz/622MHz reference clock generator IC designed for system clock distribution and frequency synchronization in OC-48 and OC-192 SONET/SDH and WDM transmission systems. The MAX3670 integrates a phase/frequency detector, an operational amplifier (op amp), prescaler dividers and input/output buffers. Using an external VCO, the MAX3670 can be configured easily as a phase-lock loop with bandwidth programmable from 15Hz to 20kHz. The MAX3670 operates from a single +3.3V or +5.0V supply, and dissipates 150mW (typ) at 3.3V. The operating temperature range is from -40°C to +85°C. The chip is available in a 5mm x 5mm, 32-pin QFN package.

II. Manufacturing Information

| | |
|----------------------------------|------------------------------------------|
| A. Description/Function: | Low-Jitter 155MHz/622MHz Clock Generator |
| B. Process: | GST2 |
| C. Number of Device Transistors: | 2478 |
| D. Fabrication Location: | Oregon |
| E. Assembly Location: | China, Thailand |
| F. Date of Initial Production: | September 28, 2001 |

III. Packaging Information

| | |
|--------------------------------------------------------------------------|--------------------------|
| A. Package Type: | 32-pin TQFN 5x5 |
| B. Lead Frame: | Copper |
| C. Lead Finish: | 100% matte Tin |
| D. Die Attach: | Conductive |
| E. Bondwire: | Au (1.3 mil dia.) |
| F. Mold Material: | Epoxy with silica filler |
| G. Assembly Diagram: | #05-9000-3411 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | 47°C/W |
| K. Single Layer Theta Jc: | 1.7°C/W |
| L. Multi Layer Theta Ja: | 29°C/W |
| M. Multi Layer Theta Jc: | 2.7°C/W |

IV. Die Information

| | |
|----------------------------|--------------------------------------------------|
| A. Dimensions: | 80 X 76 mils |
| B. Passivation: | Si ₃ N ₄ (Silicon nitride) |
| C. Interconnect: | Au |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 2 microns (as drawn) |
| F. Minimum Metal Spacing: | 2 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | SiO ₂ |
| I. Die Separation Method: | Wafer Saw |

V. Quality Assurance Information

- A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 45 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 10.93 \times 10^{-9}$$

$$\lambda = 10.93 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at <http://www.maxim-ic.com/>. Current monitor data for the GST2 Process results in a FIT Rate of 0.08 @ 25C and 1.42 @ 55C (0.8 eV, 60% UCL).

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HT17 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX3670ETJ+

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES |
|-----------------------------------------------------------|----------------------------------------------------|----------------------------------|-------------|--------------------|
| Static Life Test (Note 1) | Ta = 150°C Biased Time = 192 hrs. | DC Parameters & functionality | 45 | 0 |
| Moisture Testing (Note 2) 85/85 | Ta = 85°C RH = 85% Biased Time = 1000hrs. | DC Parameters & functionality | 77 | 0 |
| Mechanical Stress (Note 2) Temperature Cycle | -65°C/150°C 1000 Cycles Method 1010 | DC Parameters & functionality | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data