RELIABILITY REPORT

FOR

MAX6364PUTxx

PLASTIC ENCAPSULATED DEVICES

April 17, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX6364P successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. Summary

The MAX6364P supervisory circuit reduces the complexity and number of components required for power-supply monitoring and battery control functions in microprocessor (µP) systems. The circuit significantly improves system reliability and accuracy compared to that obtainable with separate ICs or discrete components. Its function includes µP reset, backup battery switchover, and power failure warning.

The MAX6364P operates from supply voltages as low as +1.2V. The factory-preset reset threshold voltage ranges from 2.32V to 4.63V. This device provides an auxiliary adjustable reset input. In addition, the part is offered in three reset output versions: an active-low push-pull reset, an active-low open-drain reset, and an active-high open-drain reset.

B. Absolute Maximum Ratings

Item	Rating
VCC, BATT, OUT to GND	-0.3V to +6V
/RESET (open drain), RESET (open drain)	-0.3V to +6V
BATT ON, /RESET (push-pull), RESET IN, WDI	-0.3V to (VOUT + 0.3V)
/MR	-0.3V to (VCC + 0.3V)
Input Current	
VCC Peak	1A
VCC Continuous	250mA
BATT Peak	250mA
BATT Continuous	40mA
GND	75mA
Output Current	
OUT	Short-Circuit Protection for up to 10s
RESET, /RESET, BATT ON	20mA
Operating Temp Range	-40^0C to $+85^0$C
Storage Temp Range	-65^0C to $+150^0$C
Junction Temperature	$+150^0$C
Lead Temp Range (soldering, 10s)	$+300^0$C
Continuous Power Dissipation (TA = $+70^0$)	
6-Pin SOT23	696mW
Derates above +70°C	
6-Pin SOT23	8.70mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Power uP Supervisory Circuit with Battery Backup
B. Process:	S8
C. Number of Device Transistors:	720
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia, Thailand
F. Date of Initial Production:	January, 2000

III. Packaging Information

A. Package Type:	**6-Pin SOT23**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1601-0090
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity Per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	57 x 35 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliablity Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 160 \times 2}$$ (Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 6.79 \times 10^{-9}$ $\lambda = 6.79$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5517) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The MS35-10 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX6364PUTxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic package/process data

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

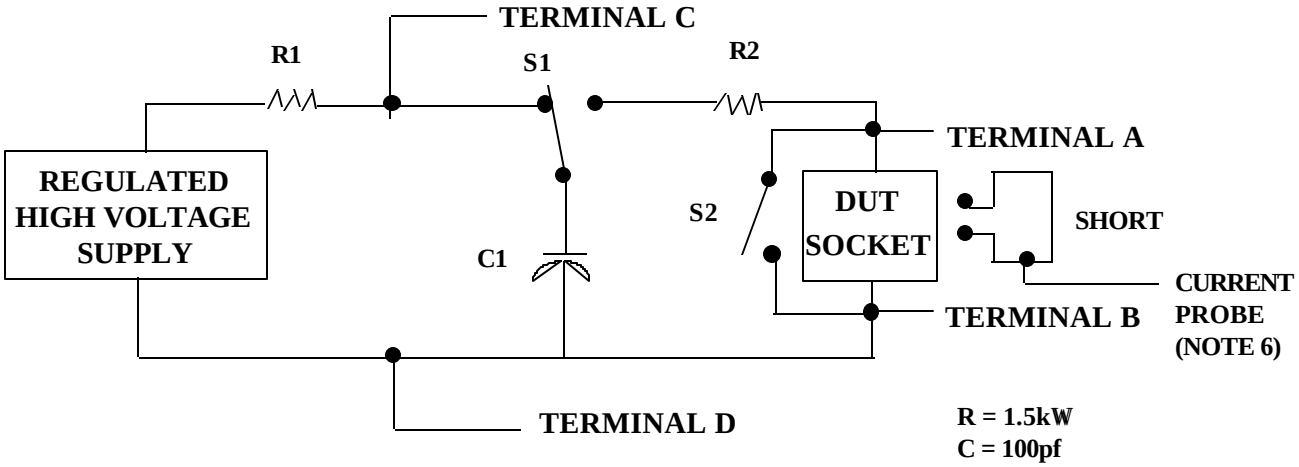
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

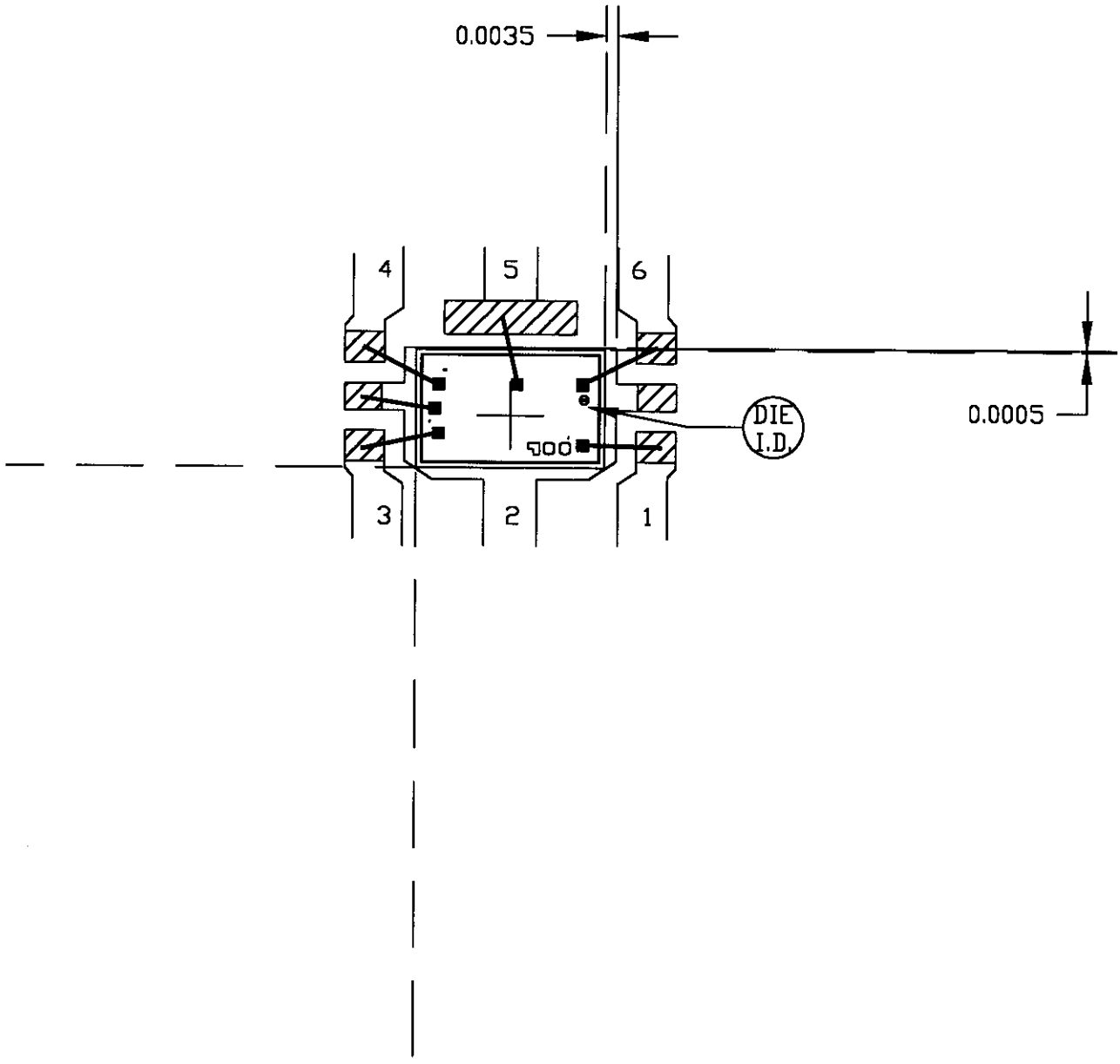
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

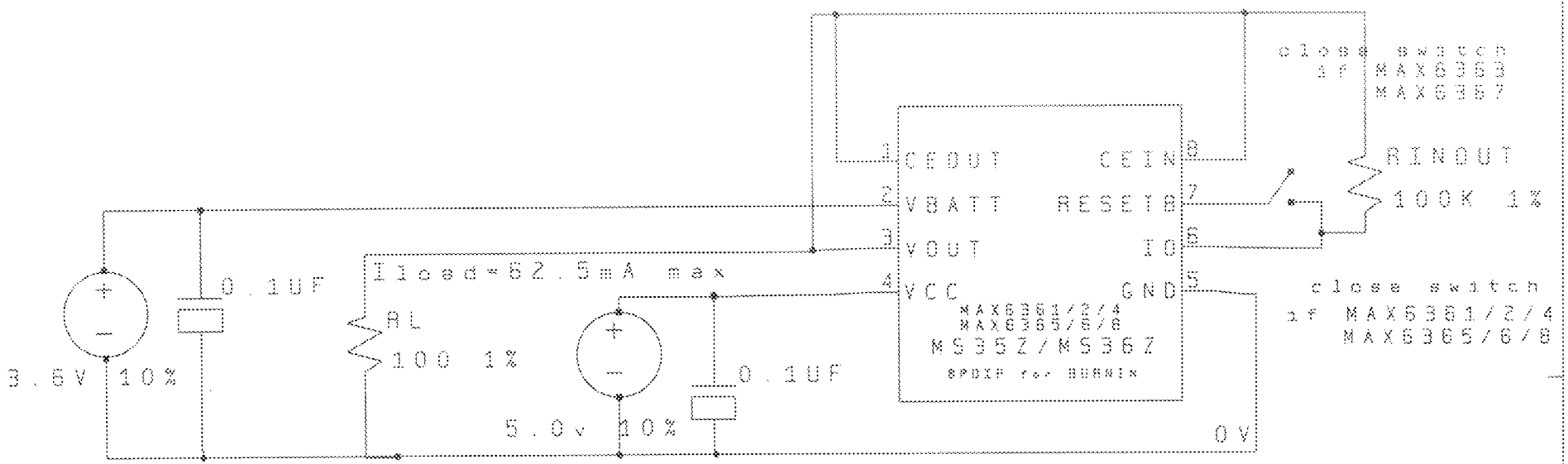




NOTE: CAVITY DOWN

PKG.CODE: U6-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 64x39	PKG. DESIGN			BUILDSHEET NUMBER: 05-1601-0090 / REV.: A

MS35Z/MS36Z BURN-IN SCHEMATIC
for MAX6361/2/4 & MAX6365/6/8



MAX6361/5 IO=/MR\ (input)
MAX6362/6 IO=WDI (input)
MAX6363/7 IO=BATT ON (output)
MAX6364/8 IO=RESET IN (input

Total Chip Power Dissipation Max 25mW
Total External Resistor Power Dissipation Max 308mW
8 PDIP for Burn In

MAXIM CONFIDENTIAL	CREATED: 00/00/00	BY: ET			ENG: -
	LAST SAVED: 8-24-1999_11:45		SIZE A	REVISION 00/00/00	DWG NO: - 06-5517 MAX6361/2/4/5/6/8
MS35Z/MS36Z BURN IN 1	PROJECT: MS35Z/MS36Z				
	DESC: MAX6361/2/4,5/6/8		FILE: MS35BI1		SHEET 1 OF 1