

RELIABILITY REPORT
FOR
MAX6501UKxxxx
PLASTIC ENCAPSULATED DEVICES

May 13, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX6501 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX6501 low-cost, fully integrated temperature switch asserts a logic signal when its die temperature crosses a factory-programmed threshold. Operating from a +2.7V to +5.5V supply, this device features two on-chip, temperature-dependent voltage references and a comparator. It is available with factory-trimmed temperature trip thresholds from -45°C to +115°C in 10°C increments, and is accurate to ±0.5°C (typ) or ±6°C (max). This device requires no external components and typically consumes 30µA supply current. Hysteresis is pin-selectable at +2°C or +10°C.

The MAX6501 has an active-low, open-drain output intended to interface with a microprocessor (µP) reset input. The MAX6501 is offered with hot-temperature thresholds (+35°C to +115°C), asserting when the temperature is above the threshold.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Supply Voltage (V_{CC})	-0.3V to +7V
/TOVER	-0.3V to +7V
All Other Pins	-0.3V to ($V_{CC} + 0.3V$)
Input Current (all pins)	20mA
Output Current (all pins)	20mA
Storage Temp.	-65°C to +165°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (+70°C)	
5-Pin SC70	571mW
Derates above +70°C	
5-Pin SC70	7.1mW/°C

II. Manufacturing Information

A. Description/Function:	Low-Cost, +2.7V to +5.5V, Micropower Temperature Switch
B. Process:	S3 ((SG3) - Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	237
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia or Thailand
F. Date of Initial Production:	September, 1997

III. Packaging Information

A. Package Type:	5 Lead SOT-23
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-1601-0028
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	38 x 57 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 270 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 4.02 \times 10^{-9} \quad \lambda = 4.02 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5186) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The MS12 die type has been found to have all pins able to withstand a transient pulse of $\pm 1000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 200\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX6501UKxxxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	270	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic package/process data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

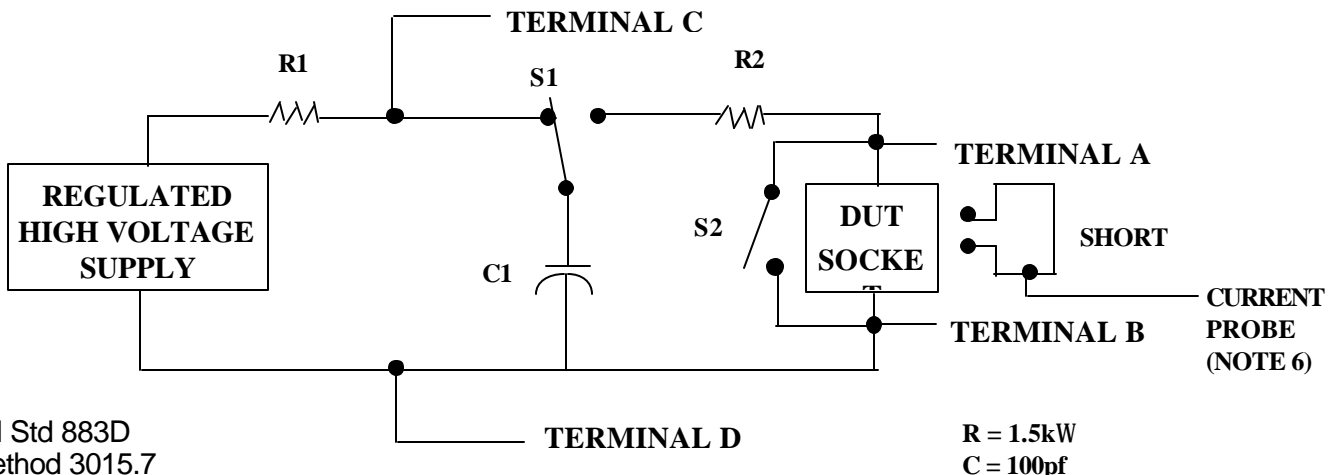
2/ No connects are not to be tested.

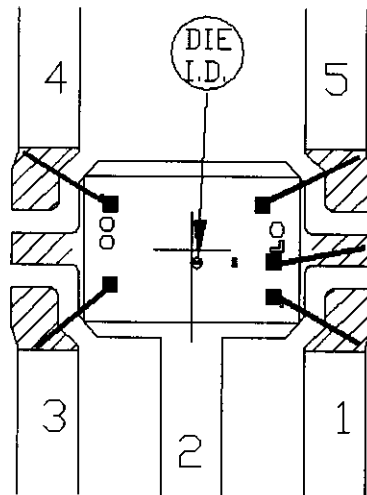
3/ Repeat pin combination I for each named Power supply and for ground


(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.

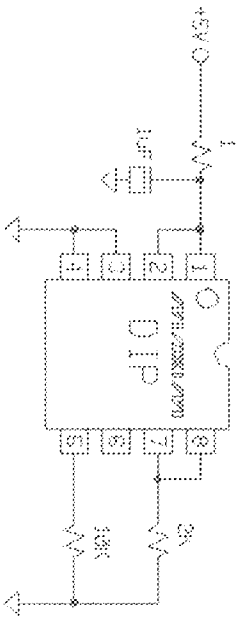




PKG.CODE: U5-2		APPROVALS	DATE	
CAV./PAD SIZE: 59X46	PKG. DESIGN			

ONCE PER DEVICE

ONCE PER BOARD



...STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
 ...BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 168 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 125C CONTINUOUS
4. APPROVED FOR (X) COMMERCIAL
 (X) MP/882

SPEC. NO. 06-5186 REV. A

MAXIM BURN-IN SCHEMATIC

DATE: 3/04/96

DEVICE TYPE(s):

MAX991/2/3

GROUND

CLK4 FREQ= 4ppm

CLK3 FREQ= AMPm

CLK2 FREQ= AMPm

CLK1 FREQ= AMPm

CLK0 FREQ= AMPm

PS6 1 =

PS5 1 =

PS4 1 =

PS3 1 =

PS2 1 =

+5V 1 < 3mA

470pF