RELIABILITY REPORT

FOR

**MAX807NxxE**

PLASTIC ENCAPSULATED DEVICES

November 19, 2002

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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**Conclusion**

The MAX807N successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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## I. Device Description

### A. General

The MAX807 microprocessor (µP) supervisory circuit reduces the complexity and number of components needed to monitor power-supply and battery-control functions in µP systems. A 70µA supply current makes the MAX807 ideal for use in portable equipment, while a 2ns chip-enable propagation delay and 250mA output current capability (20mA in battery-backup mode) make it suitable for larger, higher-performance equipment. The MAX807 provides the following functions:

1) µP reset. The active-low RESET output is asserted during power-up, power-down, and brownout conditions, and is guaranteed to be in the correct state for $V_{CC}$ down to 1V.
2) Active-high RESET output.
3) Manual-reset input.
4) Two-stage power-fail warning. A separate low-line comparator compares $V_{CC}$ to a threshold 52mV above the reset threshold. This low-line comparator is more accurate than those in previous µP supervisors.
5) Backup-battery switchover for CMOS RAM, real-time clocks, µPs, or other low-power logic.
6) Write protection of CMOS RAM or EEPROM.
7) 2.275V threshold detector provides for power-fail warning and low-battery detection, or monitors a power supply other than +5V.
8) BATT OK status flag indicates that the backup-battery voltage is above 2.275V.
9) Watchdog-fault output—asserted if the watchdog input has not been toggled within a preset time-out period.

### B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| Input Voltages (with respect to GND) | |
| $V_{CC}$ | -0.3V to 6V |
| $V_{BATT}$ | -0.3V to 6V |
| All Other Inputs | -0.3V to (VOUT + 0.3V) |
| Input Current | |
| $V_{CC}$ Peak | 1.0A |
| $V_{CC}$ Continuous | 500mA |
| $I_{BATT}$ Peak | 250mA |
| $I_{BATT}$ Continuous | 50mA |
| GND | 50mA |
| All Other Inputs | 50mA |
| Storage Temp. | -65°C to +160°C |
| Lead Temp. (10 sec.) | +300°C |
| Continuous Power Dissipation (TA = +70°C) | |
| 16-Pin Plastic DIP | 842mW |
| 16-Pin WSO | 762mW |
| 16-Pin TSSOP | 533mW |
| Derate above +70°C | |
| 16-Pin Plastic DIP | 10.53mW/°C |
| 16-Pin WSO | 9.52mW/°C |
| 16-Pin TSSOP | 6.70mW/°C |

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | Full-Featured µP Supervisory Circuit with ±1.5% Reset Accuracy |
| B. Process: | S3 (Standard 3 micron silicon gate CMOS) |
| C. Number of Device Transistors: | 984 |
| D. Fabrication Location: | Oregon, USA |
| E. Assembly Location: | Philippines or Malaysia |
| F. Date of Initial Production: | September, 1995 |

## III. Packaging Information

| | | | |
|---|---|---|---|
| A. Package Type: | 1**6 Lead WSO** | **16 Lead PDIP** | **16 TSSOP** |
| B. Lead Frame: | Copper | Copper | Copper |
| C. Lead Finish: | Solder Plate | Solder Plate | Solder Plate |
| D. Die Attach: | Silver-filled Epoxy | Silver-filled Epoxy | Silver-filled Epoxy |
| E. Bondwire: | Gold (1.3 mil dia.) | Gold (1.3 mil dia.) | Gold (1.0 mil dia.) |
| F. Mold Material: | Epoxy with silica filler | Epoxy with silica filler | Epoxy with silica filler |
| G. Assembly Diagram: | #05-1701-0256 | #05-1701-0255 | #05-1701-0350 |
| H. Flammability Rating: | Class UL94-V0 | Class UL94-V0 | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: | Level 1 | Level 1 | Level 1 |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 100 x 124 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Si (Si = 1%) |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 3 microns (as drawn) |
| F. Minimum Metal Spacing: | 3 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

A. Quality Assurance Contacts: Michael Herman (Director of Reliability)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-9}$

$\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5137) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PW49-2 die type has been found to have all pins able to withstand a transient pulse of ±600V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±200mA and/or ±20V.

**Table 1**
Reliability Evaluation Test Results
**MAX807NxxE**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 80 | 0 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 96hrs. | DC Parameters<br>& functionality | PDIP<br>WSO<br>TSSOP | 77<br>77 | 0<br>0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters | | 77 | 0 |

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

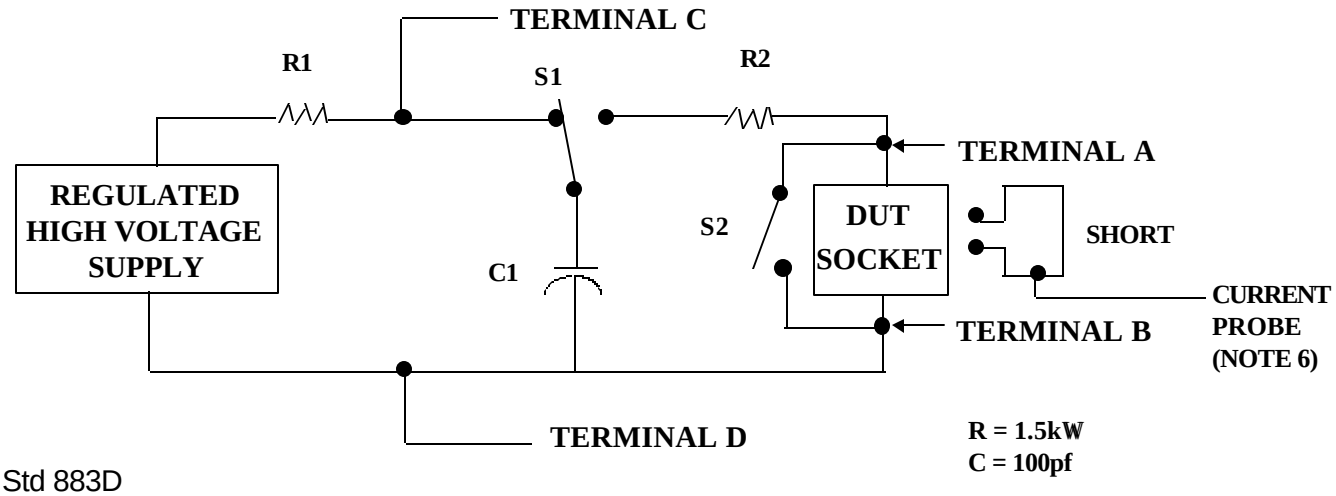
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

3.4 Pin combinations to be tested.

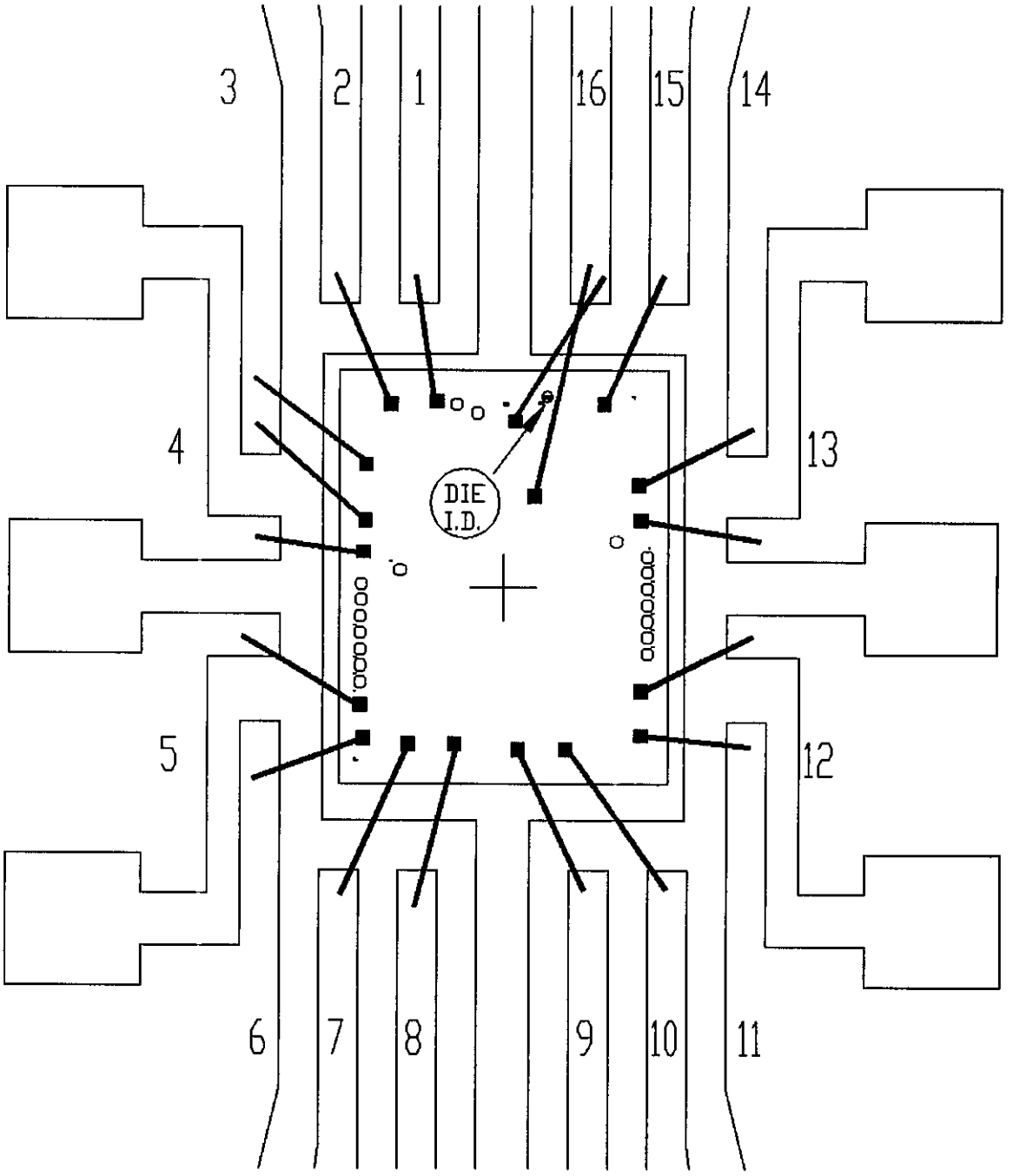
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

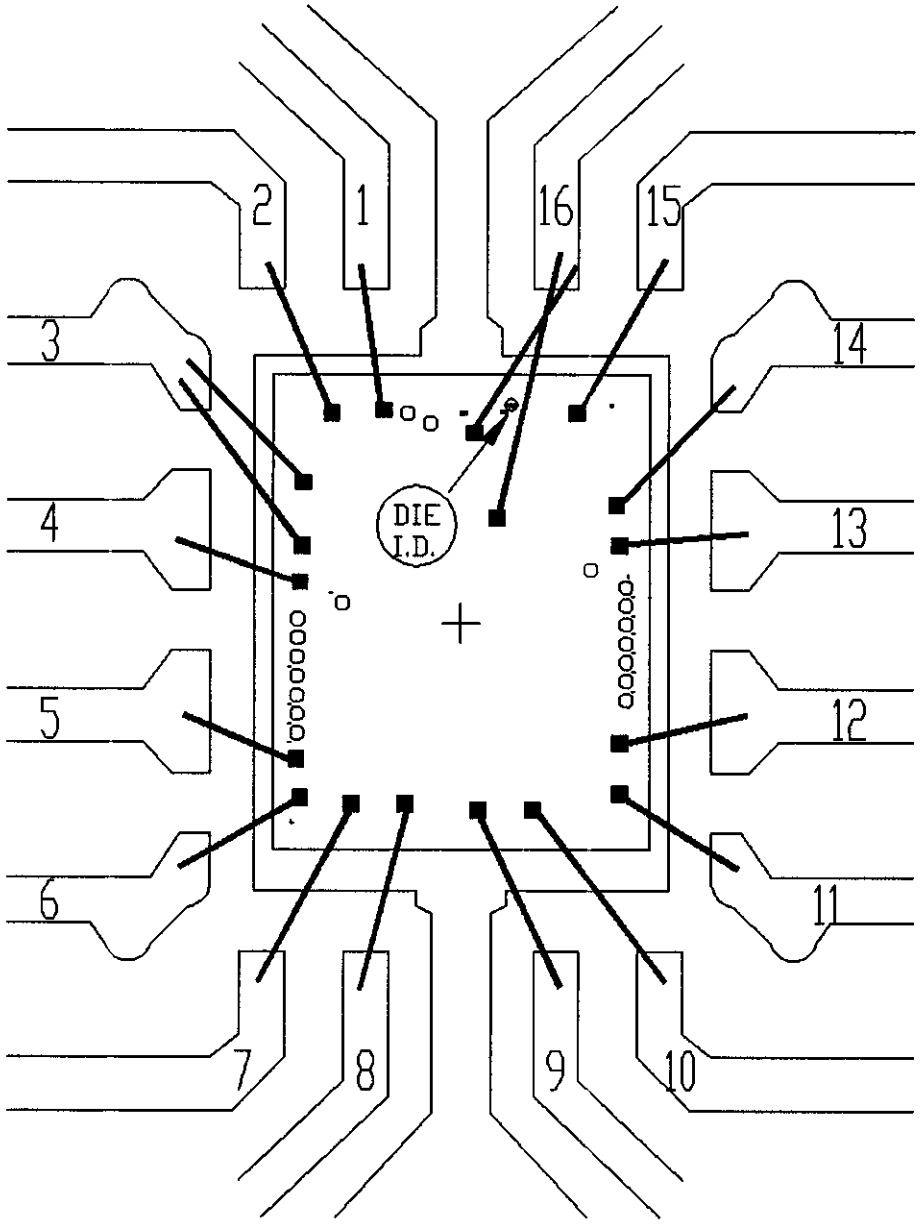
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



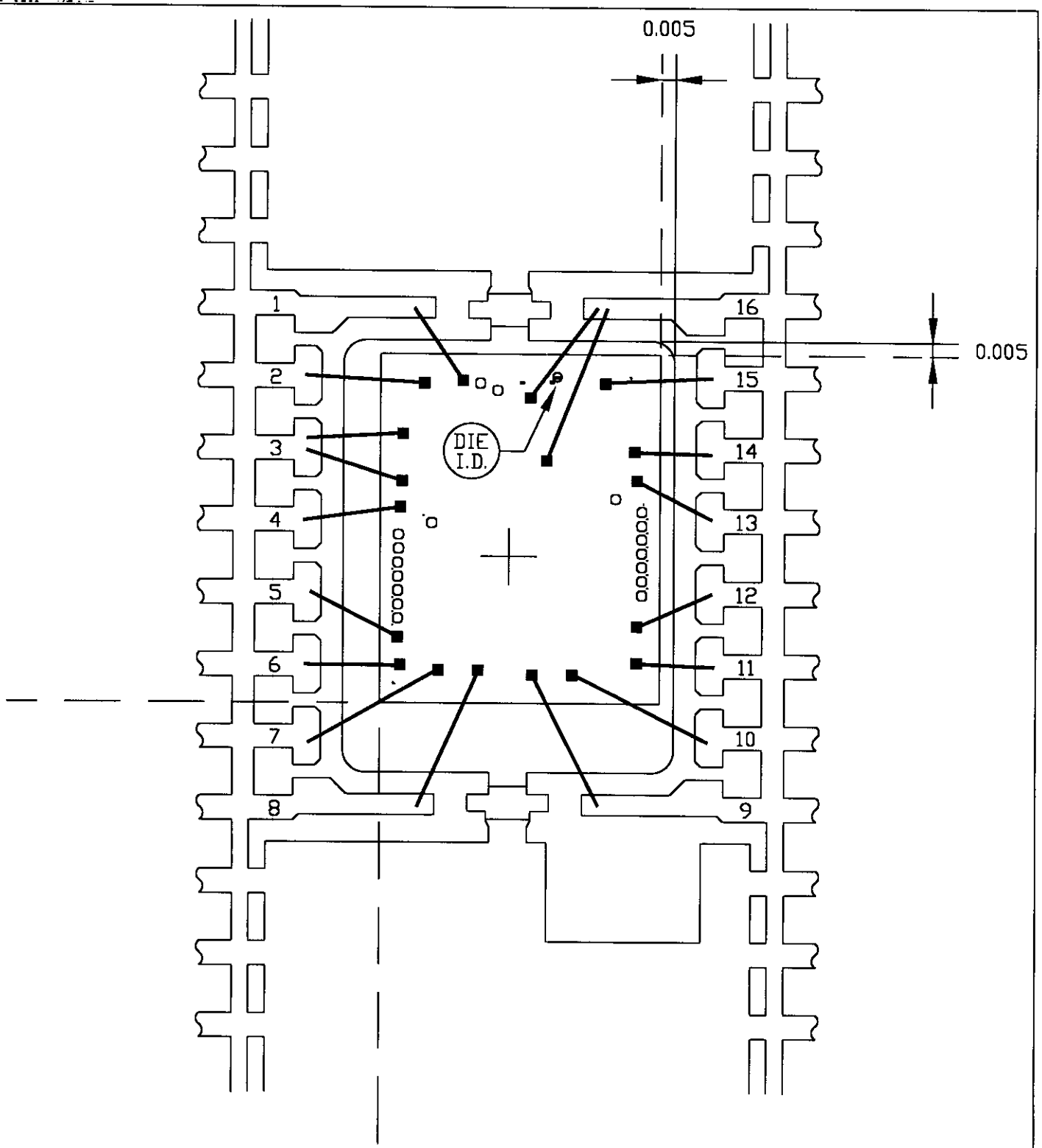

Mil Std 883D
Method 3015.7
Notice 8



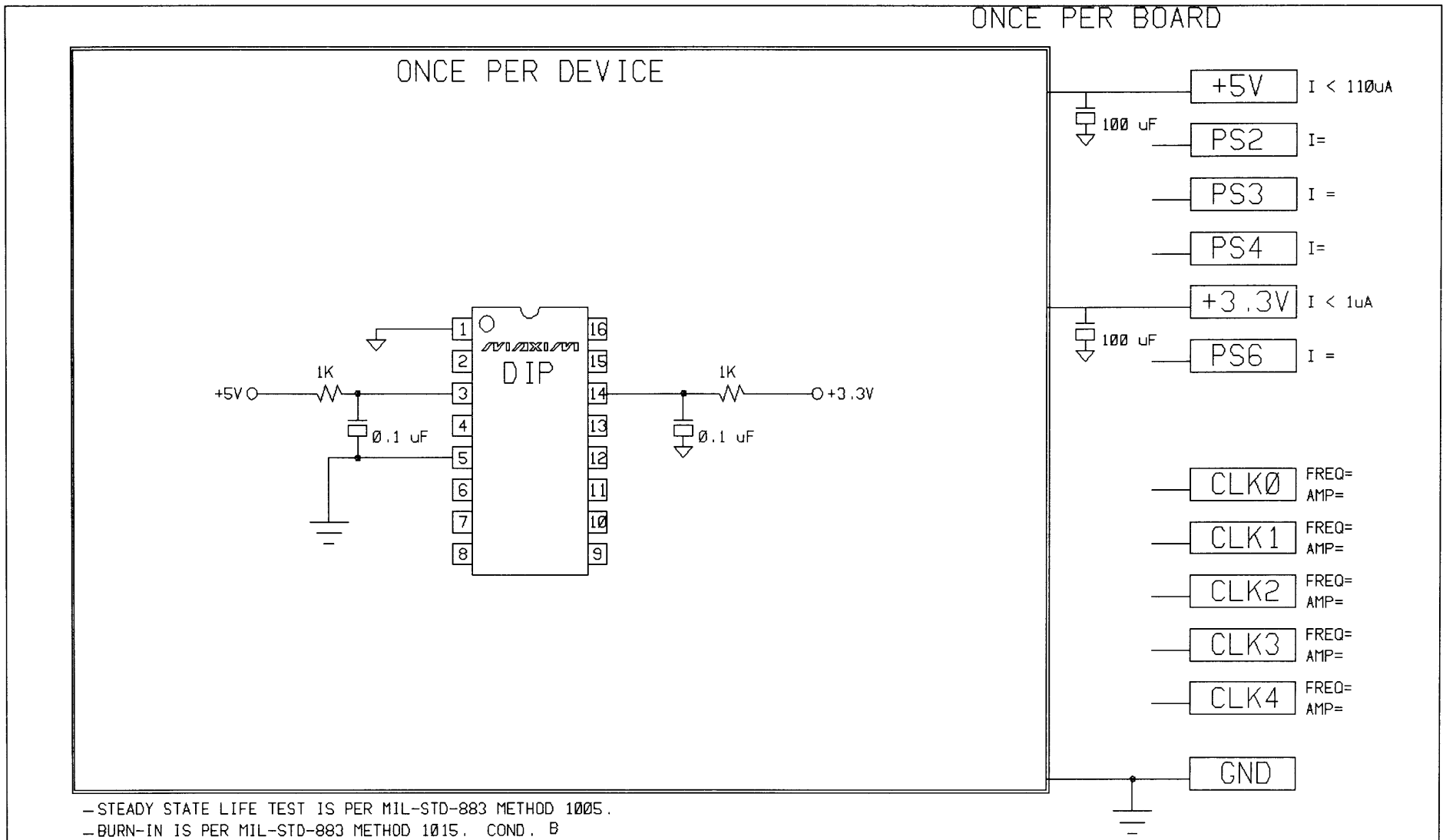

| | | | | |
|---|---|---|---|---|
| PKG.CODE: P16-1 | | APPROVALS | DATE | MAXIM |
| CAV./PAD SIZE: 110 X 140 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-1701-0255 / REV.: A |




| PKG.CODE: W16-1 | | APPROVALS | DATE | MAXIM | |
|---|---|---|---|---|---|
| CAV./PAD SIZE: 110 X 140 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-1701-0256 | REV.: A |




| | | | | |
|---|---|---|---|---|
| PKG.CODE: U16-1 | | APPROVALS | DATE | MAXIM |
| CAV./PAD SIZE: 118X154 | PKG. DESIGN | | | BUILDSHEET NUMBER: 05-1701-0350 / REV.: A |




NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] HR/883

SPEC. NO. 06-5137 REV: A

DATE: 8/30/95

DRAWN BY:

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE(S):

MAX807