

RELIABILITY REPORT
FOR
MAX868EUB
PLASTIC ENCAPSULATED DEVICES

June 24, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
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Conclusion

The MAX868 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX868 inverting charge pump provides a low-cost and compact means of generating a regulated negative voltage up to $-2 \times V_{IN}$ from a positive input voltage between 1.8V and 5.5V. It uses a pulse-frequency-modulation (PFM) control scheme to generate the regulated negative output voltage. PFM operation is obtained by gating the internal 450kHz oscillator on and off as needed to maintain output voltage regulation. This unique on-demand switching scheme gives the MAX868 excellent light-load efficiency without degrading its full-load operation (up to 30mA), permitting smaller capacitors to take advantage of the oscillator's high switching frequency.

The MAX868 requires no inductors; only four capacitors are required to build a complete DC-DC converter. Output voltage regulation is achieved by adding just two resistors. The MAX868 comes in a 10-pin μ MAX package, which is only 1.11mm high and occupies just half the board area of a standard 8-pin SO.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
IN to GND	-0.3V to +6V
OUT to GND	+0.3V to -12V
IN to OUT	-0.3V to -17V
C1+ to GND	$(V_{IN} - 12V)$ to $(V_{IN} + 0.3V)$
C1- to GND	+0.3V to -12V
C2+ to GND	$(V_{IN} + 0.3V)$ to -6V
C2- to GND	+0.3V to -6V
/SHDN, FB to GND	-0.3V to $(V_{IN} + 0.3V)$
PGND to GND	-0.3V to +0.3V
Output Current	35mA
Short-Circuit Duration	Continuous
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
10-Pin μ MAX	330mW
Derates above +70°C	
10-Pin μ MAX	5.6mW/°C

II. Manufacturing Information

A. Description/Function:	Regulated, Adjustable -2x Inverting Charge Pump
B. Process:	SG5 (Standard 5 micron silicon gate CMOS)
C. Number of Device Transistors:	96
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Malaysia, Thailand or Philippines
F. Date of Initial Production:	October, 1997

III. Packaging Information

A. Package Type:	10-Lead mMAX
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-1101-0047
H. Flammability Rating:	Class UL94-V0

IV. Die Information

A. Dimensions:	61 x 87 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	5 microns (as drawn)
F. Minimum Metal Spacing:	5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 155 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 7.01 \times 10^{-9} \quad \lambda = 7.01 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5289) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PX25 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 100\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX868EUB

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		155	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uMAX	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

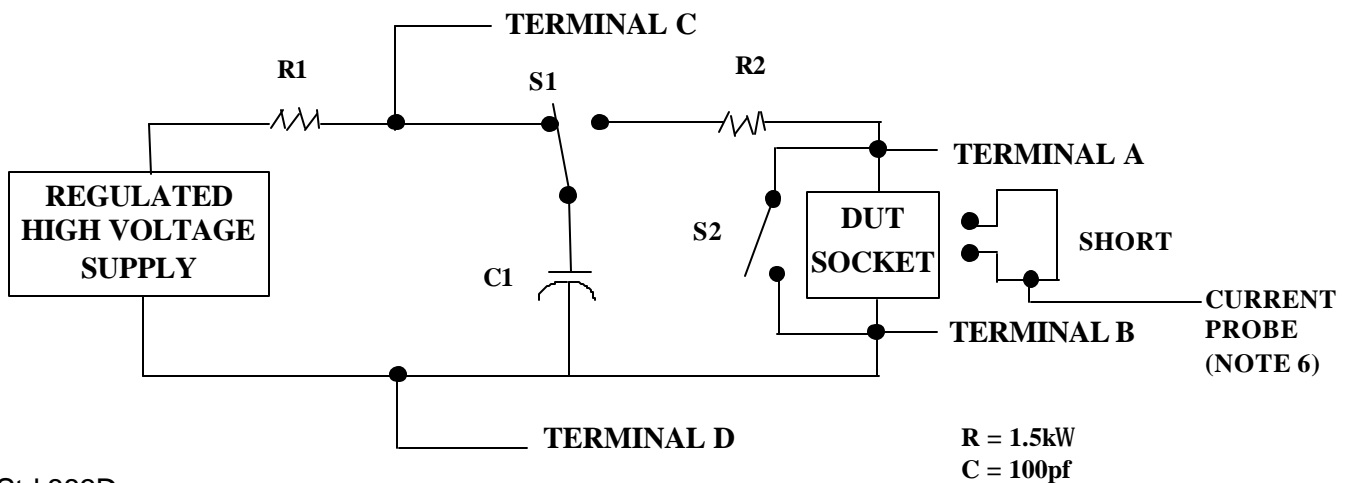
2/ No connects are not to be tested.

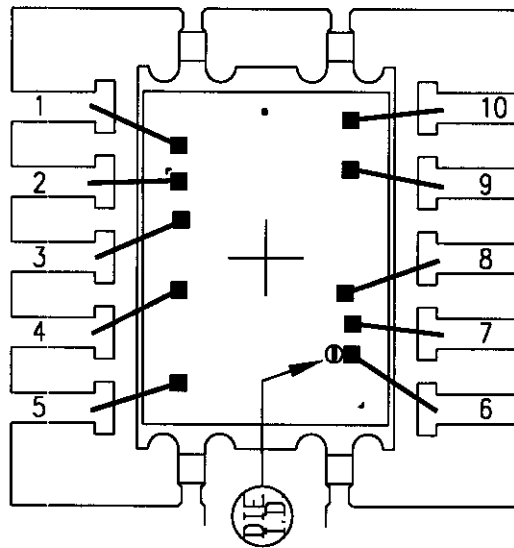
3/ Repeat pin combination I for each named Power supply and for ground


(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: U10-2		APPROVALS	DATE		
CAV./PAD SIZE: 68X94	PKG. DESIGN			BUILDSHEET NUMBER: 05-1101-0047	REV.: B

