RELIABILITY REPORT

FOR

MAX9225ETE+

PLASTIC ENCAPSULATED DEVICES

March 19, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Conclusion

The MAX9225ETE+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

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I. Device Description

A. General

The MAX9225/MAX9226 serializer/deserializer chipset reduces wiring by serializing 10 bits onto a single differential pair. Ten bits are serialized in each cycle of the parallel input clock resulting in a 100Mbps to 200Mbps net serial-data rate. The MAX9225 serializes the 8-bit YUV, HSYNC, and VSYNC outputs from a camera mounted in the flip part of the phone, reducing wiring through the hinge to the baseband processor in the base of the phone. The 2-wire serial interface uses low-current differential signaling (LCDS) for low EMI, high common-mode noise immunity, and ground-shift tolerance. The MAX9225/MAX9226 automatically identify the word boundary in the serial data in case of signal interruption. The MAX9226 power-down is controlled by the MAX9225. The MAX9225/MAX9226 consume 3.5µA or less in power-down mode. The MAX9225 serializer operates from a single +2.375V to +3.465V supply and accepts +1.71V to +3.465V inputs. The MAX9226 deserializer operates from a +2.375V to +3.465V core supply and has a separate output buffer supply (VDDO), allowing +1.71V to +3.465V output high levels. The MAX9225/MAX9226 are specified over the -40°C to +85°C extended temperature range and are available in 16-pin TQFN (3mm x 3mm x 0.8mm) packages with an exposed paddle.

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II. Manufacturing Information

A. Description/Function:	10-Bit, Low-Power, 10MHz-to-20MHz Serializer and Deserializer Chipset
B. Process:	TS35
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	China, Malaysia, Philippines, Thailand
F. Date of Initial Production:	January 20, 2006

III. Packaging Information

A. Package Type:	16-pin TQFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2013
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	64°C/W
K. Single Layer Theta Jc:	6.9°C/W
L. Multi Layer Theta Ja:	48°C/W
M. Multi Layer Theta Jc:	6.9°C/W

IV. Die Information

A. Dimensions:	61 X 61 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35µm
F. Minimum Metal Spacing:	0.35µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Ken Wendel (Director, Reliability Engineering)
Bryan Preeshl (Managing Director of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

λ = 22.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim"s reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS35 Process results in a FIT Rate of 0.11 @ 25C and 1.93 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HS34-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

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Table 1
Reliability Evaluation Test Results

MAX9225ETE+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
HAST	Ta = 130°C RH = 85% Biased Time = 96hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

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