RELIABILITY REPORT

FOR

MAX9248

PLASTIC ENCAPSULATED DEVICES

June 23, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX9248ECM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX9248/MAX9250 digital video serial-to-parallel converters deserialize a total of 27 bits during data and control phases. In the data phase, the LVDS serial input is converted to 18 bits of parallel video data and in the control phase, the input is converted to 9 bits of parallel control data. The separate video and control phases take advantage of video timing to reduce the serial-data rate. The MAX9248/MAX9250 pair with the MAX9247 serializer to form a complete digital video transmission system. For operating frequencies less than 35MHz, the MAX9248/MAX9250 can also pair with the MAX9217 serializer. The MAX9248 features spread-spectrum capability, allowing output data and clock to spread over a specified frequency range to reduce EMI. The data and clock outputs are programmable for a spectrum spread of ±4% or ±2%. The MAX9250 features output enable input control to allow data busing. Proprietary data decoding reduces EMI and provides DC balance. The DC balance allows AC-coupling, providing isolation between the transmitting and receiving ends of the interface. The MAX9248/MAX9250 feature a selectable rising or falling output latch edge. ESD tolerance is specified for ISO 10605 with ±10kV Contact Discharge and ±30kV Air-Gap Discharge. The MAX9248/MAX9250 operate from a +3.3V ±10% core supply and feature a separate output supply for interfacing to 1.8V to 3.3V logic-level inputs. These devices are available in a 48-lead LQFP package and are specified from -40°C to +85°C or -40°C to +105°C.

II. Manufacturing Information

A. Description/Function:	27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers
B. Process:	0.35UM 2 Poly 3 Metal CMOS
C. Number of Device Transistors:	85,535
D. Fabrication Location:	Taiwan (TSMC Foundry)
E. Assembly Location:	Malaysia and Korea
F. Date of Initial Production:	January 21, 2006

III. Packaging Information

A. Package Type:	48-pin LQFP
B. Lead Frame:	Copper
C. Lead Finish:	100% Matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2191
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	46°C/W
M. Multi Layer Theta Jc:	10°C/W

IV. Die Information

A. Dimensions:	134 X 117 mils
B. Passivation:	Silicon Dioxide / Silicon Nitride
C. Interconnect:	Al/0.5%Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35u
F. Minimum Metal Spacing:	0.35u
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	Silicon Dioxide
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135c biased (static) life test are pending. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.91 \times 10^{-9}$

$\lambda = 22.91$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim"s reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6629) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (RR-1N). Current monitor data for the TSMC Process results in a FIT Rate of 0.1 @ 25C and 1.75 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The HS48 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA, 1.5x VCCMax Overvoltage per Jedec JESD78.

Table 1
Reliability Evaluation Test Results

MAX9248

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135c Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data