

RELIABILITY REPORT  
FOR  
**MAX999EUK**  
PLASTIC ENCAPSULATED DEVICES

April 15, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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## Conclusion

The MAX999 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX999 is a low-power, ultra-high-speed comparators with internal hysteresis. This device is optimized for single +3V or +5V operation. The input common-mode range extends 100mV Beyond-the-Rails™, and the outputs can sink or source 4mA to within 0.52V of GND and Vcc. Propagation delay is 4.5ns (5mV overdrive), while supply current is 5mA per comparator.

The MAX999 is available in a tiny SOT23-5 package.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Supply Voltage, VCC to GND	-0.3V to +6V
All Other Pins	-0.3V to (VCC + 0.3V)
Duration of Output Short Circuit to GND or VCC	Continuous
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (soldering, 10sec)	+300°C
Continuous Power Dissipation (TA = +70°C)	
5-Pin SOT23	571mW
Derates above +70°C	
5-Pin SOT23	7.1mW/°C

## II. Manufacturing Information

- A. Description/Function: Single/Dual/Quad, Ultra-High-Speed, +3V/+5V, Beyond-the-Rails Comparators
- B. Process: CB20 - Complementary Bipolar Process
- C. Number of Device Transistors: 142
- D. Fabrication Location: Oregon, USA
- E. Assembly Location: Malaysia or Thailand
- F. Date of Initial Production: January, 1998

## III. Packaging Information

- A. Package Type: **5-Lead SOT23**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate
- D. Die Attach: Silver-filled Epoxy
- E. Bondwire: Gold (1.0 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: # 05-1501-0147
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

## IV. Die Information

- A. Dimensions: 57 x 33 mils
- B. Passivation:  $\text{Si}_3\text{N}_4/\text{SiO}_2$  (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Gold
- D. Backside Metallization: None
- E. Minimum Metal Width: 2 microns (as drawn)
- F. Minimum Metal Spacing: 2 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric:  $\text{iO}_2$
- I. Die Separation Method: Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Rel Operations)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 159 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└ Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 6.83 \times 10^{-9} \quad \lambda = 6.83 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5374) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The CM40 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2000\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX999EUK**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		159	0
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

## Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

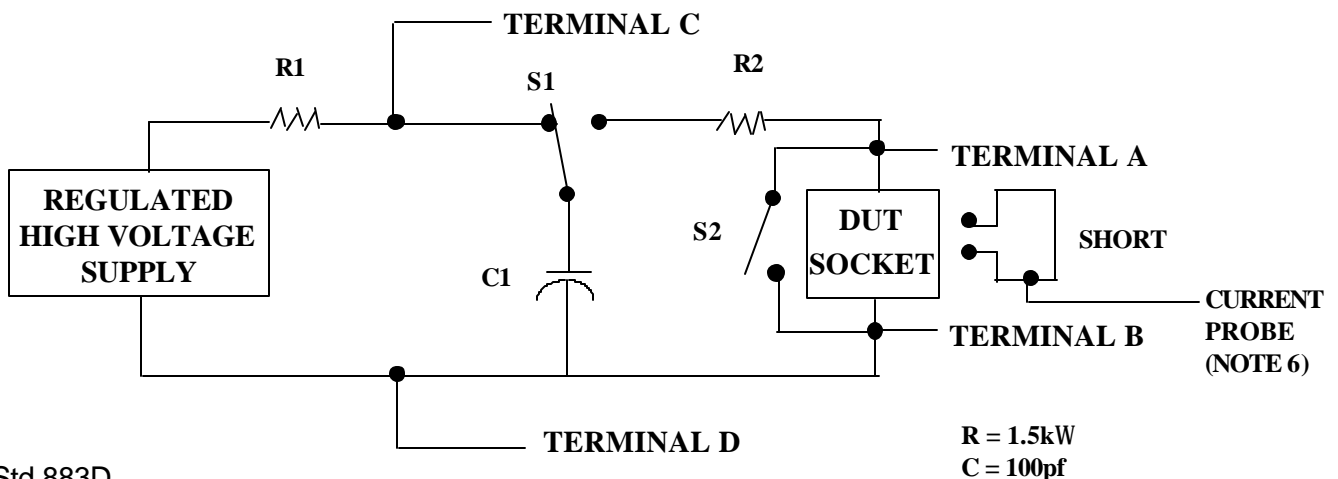
2/ No connects are not to be tested.

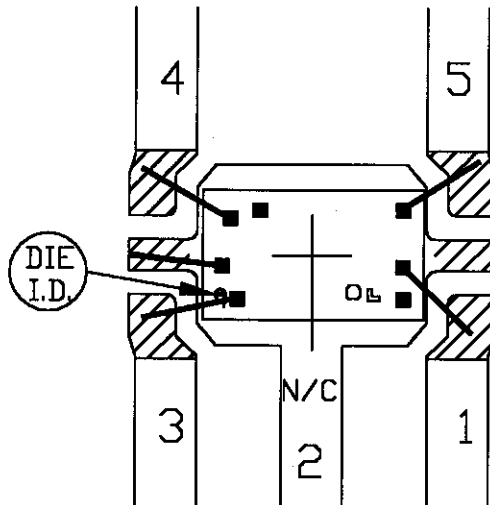
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

### 3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE:	U5-2		APPROVALS	DATE	<b>MAXIM</b>
CAV./PAD SIZE:	59X46	PKG. DESIGN			
					REV.: A

