

## MAX3272 I/O Model

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Components*.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

Version A1, May 18, 2003

## MAX3272 2.5Gbps Limiting Amplifier

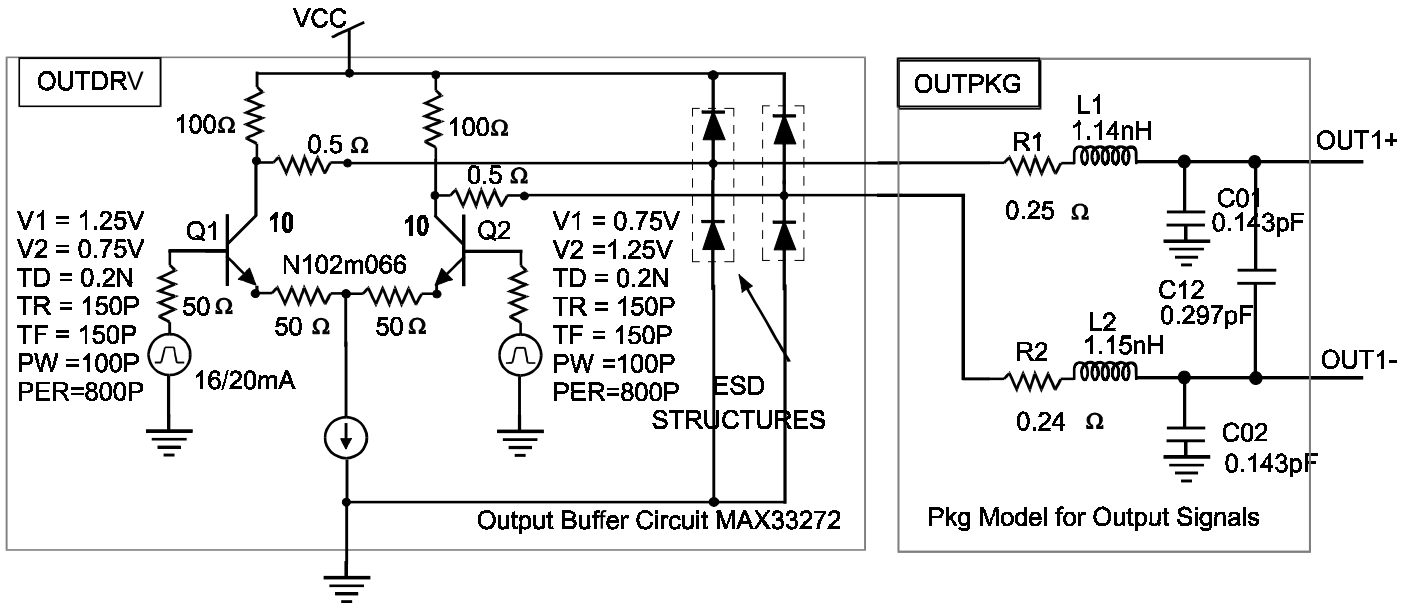


Figure 1. Output signal buffer for the MAX3272 including a simplified package model.

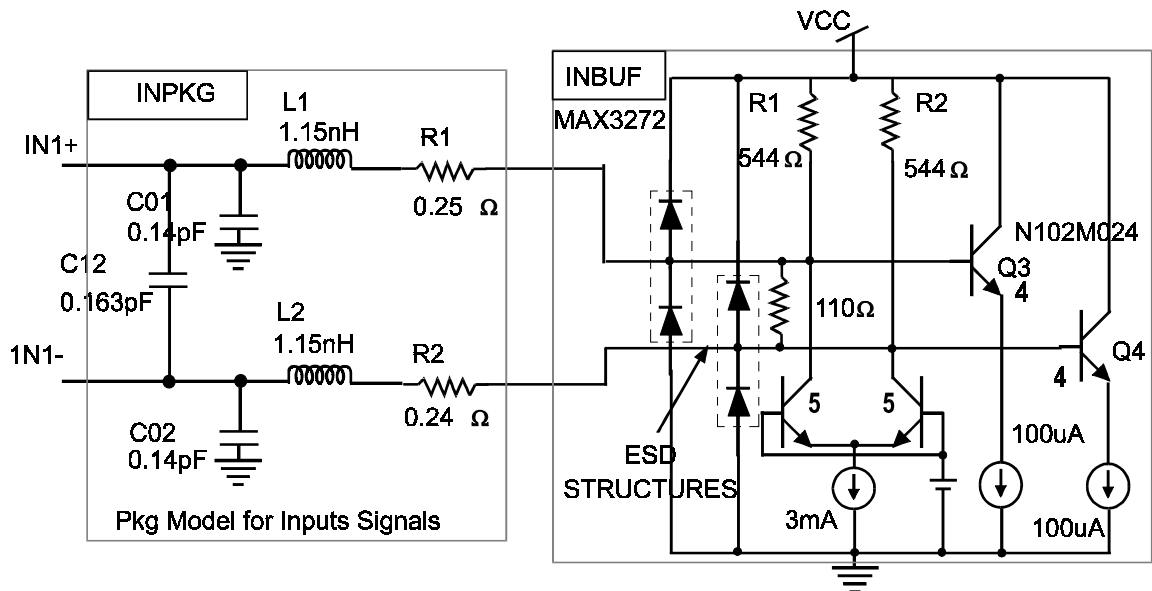


Figure 2. Simplified input package model and input circuitry for the MAX3272.

## Notes:

### MAX3272 Input Model

The input structure of the MAX3272 is connected to a differential common-emitter amplifier that is designed to compensate for internal device mismatches. In the actual circuit there is a feedback path that controls the differential amplifier to adjust the input biasing points and compensate for any device mismatch. This model does not attempt to model the offset correction functionality, but the amplifier is included to account for any parasitic impedance that it presents to the input pins.

The input pins are nodes 1001 (IN+) and 1002 (IN-). These are connected to a model pattern generator that includes  $50\Omega$  output impedance and AC coupling. The pattern generator has two  $1M\Omega$  resistors connected to ground to provide a DC path to ground at these nodes, which is a requirement of the Spice simulator.

The driving voltage source (VIN) should be set to 0V differential at  $t=0$ . This ensures that the two AC coupling capacitors are not charged to different voltages initially. (This is the way the circuit operates in steady-state operation.) I achieved this condition by using a piece-wise linear source as my driver, with a voltage of 0V at  $t=0$ . The swing applied to the input can be varied across the acceptable range of input for the MAX3272, which is  $10mV_{P-P}$  to  $1200mV_{P-P}$ . Remember that there is a 50% drop across the  $50\Omega$  output impedance of the generator, so to get a  $10mV_{P-P}$  swing at the input the MAX3272 the source should swing between  $+10mV$  and  $-10mV$  (a  $20mV_{P-P}$  swing).

### MAX3272 CML Output Model

The CML output model is a simplified version of the output stage used by the MAX3272 limiting amplifier. The package model is quite accurate, and the output impedance presented by the output emitter-followers should also be fairly accurate. Simplifications have been made regarding performance over temperature, so the model is only accurate at a temperature of  $35^{\circ}C$ . Operation at other temperatures will give very different results than the actual MAX3272 output. The model was not compensated for variation in VCC, so  $VCC=3.3V$  should be used.

The netlist includes the external resistors to set the termination to 50 Ohms. The output pins are nodes 2001 (OUT-) and 2002 (OUT+). The output disable function for the part is not implemented in this model.

**Text File Format:** This model is shipped in “pdf” format. Models and netlists can be copied to text format in the Acrobat Reader by holding the left mouse button on the “Text Select

Tool.” Then the user can “select” what netlist and/or subcircuit with the mouse. Then use the copy command from the “edit” menu to capture the selected lines. These lines can then be “pasted” into the user’s text file. Make sure to save the text tile as plain text without any formatting.

## Circuit Netlist – Input circuit

```
INPUT - MAX3272 INPUT CIRCUIT
*
* THIS IS THE TYPICAL INPUT OF THE MAX3272
* IN+ IS NODE 1001 AND IN- IS NODE 1002
*

.OPTIONS ACCT NOMOD NOPAGE LIMPTS=1000000 RELTOL=.001

.WIDTH OUT=80

.TEMP 82

.OP
.TRAN 2P 1.7N

* DRIVER *****
VIN 81 82 PWL(0 0 50P 600M 350P 600M 450P -600M 750P -600M 850P 600M)
R6 81 91 50
R5 82 92 50
C1 91 1001 0.1U IC=0
C2 92 1002 0.1U IC=0
R21 81 0 1MEG
R22 82 0 1MEG
*****

VCC 101 0 DC 3.3

XINPKG1 10011 10021 1001 1002 INPKG

XBUF 10011 10021 101 INBUF
.SUBCKT INBUF 1001 1002 101

XPAD1 1001 101 PADESD25
XPAD2 1002 101 PADESD25

XR1 1001 3001 0 RND272
XR2 3001 101 0 RND272
XR3 1002 3002 0 RND272
XR4 3002 101 0 RND272
XR5 1001 1002 0 RND110

XQ1a 1001 3 4 0 N102M024_4
XQ2a 1002 3 4 0 N102M024_4

XQ3a 101 1001 4001 0 N102M024_4
XQ4a 101 1002 4002 0 N102M024_4

I1 4 0 2.8M
I2 4002 0 1M
I3 4001 0 1M
VOFFSET 3 0 2
.ENDS INBUF

*****

*****

.SUBCKT N102M024_4 1 2 3 21
CP1SUB 2 201 5.199F
RP1SUB 20 201 100K
CTRENCH 1 202 22.907F
```

```

RFIELDDEPI 202 21 0.0001
RREVERT 202 20 0.00001
CBL 10 20 4.048F
RSUB 20 21 126.183K
CWAFAER 20 21 4.175F
CP1EPI 10 12 4.202F
CP1P2 12 3 4.201F
RBX 2 12 32.509 TC=2.271M
RCX 1 10 11.771 TC=2.717M,449.424N
RCI 10 11 2.943 TC=2.717M,449.424N
REX 13 3 8.599
QN 11 12 13 11 TX 4
*XREPORT1 0 REPORTERL1N6
*XREPORT2 0 REPORTERL1N7
.MODEL TX NPN( IS=2.558E-018 XTI=3 EG=1.120 BF=380 BR=12 XTB=0 VAF=66
+ VAR=2.500 NF=1.018 NR=1.020 NE=2 NC=1.560 IKF=5.628M IKR=159.900U
+ ISE=1.279E-018 ISC=0 RB=32.509 RBM=24.382 IRB=575.640U CJE=6.016F
+ MJE=463M VJE=1.100 FC=990M CJC=3.276F MJC=350M VJC=1 TFF=1.320P TR=5N
+ XTF=2 VTF=1.200 ITF=20.787M PTF=5 KF=102.378N AF=2.150 )
.ENDS N102M024_4
*****

*****
* TSPICE CONVERSION TO SPICE2G.6
*created Fri May 10 14:56:27 2002
*
*
.SUBCKT HDE113032 1 2 21
CP1EPI 1 4 88.881F
QD 5 4 1 5 QESD
RS 4 2 2.531 TC=2.729M,1.896U
RSUB 5 21 2.936K
CTRENCH 2 5 22.961F
.MODEL QESD PNP( IS=1.181E-017 NF=1.050 BF=800M BR=600U CJE=155.018F
+ VJE=600M MJE=400M CJC=53.258F VJC=650M MJC=400M )
.ENDS HDE113032
*****
*****
* TSPICE CONVERSION TO SPICE2G.6
*created Sun Mar 16 11:44:25 2003
*
*
.SUBCKT RND272 1 2 3
*Revision: 1.1 Date: 1999/10/25 16:56:08
R1 1 4 135.577 TC=150U
R2 4 2 135.577 TC=150U
C1 1 3 8.488E-016
C2 4 3 3.395F
C3 2 3 8.488E-016
*XREPORT1 0 REPORTERL1N0
*XREPORT2 0 REPORTERL1N1
* read ~/lib/gst2/generic/models/resistors/inst_rnd
.ENDS RND272
*
*
.SUBCKT RND110 1 2 3
*Revision: 1.1 Date: 1999/10/25 16:56:08
*2-section parameterized model for f60 nichrome/M2 contact resistors
*this model will accept l (drawn length), w (drawn width), and rreq
*(requested resistance at 27C) as parameters as follows:
*rex 1 2 3 rnd : rreq=400 ->calc min size resistor, round to *0.1um.
*rex 1 2 3 rnd : l=15 w=32 ->use l and w, round to 0.1um.
*rex 1 2 3 rnd : l=15 w=32 rreq=400 ->use l and w, round to 0.1um.
*rex 1 2 3 rnd : l=15 rreq=400 ->use l and rreq, compute w to *0.1um.
*rex 1 2 3 rnd : w=32 rreq=40 ->use w and rreq, compute l to *0.1um.

```

R1 1 4 54.808 TC=150U  
R2 4 2 54.808 TC=150U  
C1 1 3 6.130E-016  
C2 4 3 2.452F  
C3 2 3 6.130E-016  
\*XREPORT1 0 REPORTERL1N2  
\*XREPORT2 0 REPORTERL1N3  
\* read ~/lib/gst2/generic/models/resistors/inst\_rnd  
.ENDS RND110

\*\*\*\*\*  
\*\*\*\*\*

.SUBCKT INPKG 101 102 201 202  
\*  
\* resistors  
\*  
RB01 201 301 0.25  
RB02 202 302 0.25  
\*  
\* inductors  
\*  
LLAP\_1\_3 101 301 1.2N  
LLAP\_2\_4 102 302 1.3N  
K02\_03 LLAP\_1\_3 LLAP\_2\_4 0.294

\*LB03 PADT PADBOT 23P  
\*  
\* capacitors  
\*  
C01 101 0 143F  
C02 102 0 143F  
\*  
\* mutual capacitors  
\*  
C01\_02 101 102 43.800F

.ENDS INPKG

\*\*\*\*\*

.SUBCKT PADES25 1001 101  
XP1 1001 0 PAD4SQ3P7  
XQ1 1001 0 0 DE0172  
XQ2 0 1001 0 DE0172  
.ENDS PADES25  
\*

.SUBCKT PAD4SQ3P7 1 3  
CPAD 1 10 67.534F  
REPI 10 20 378.507 TC=4.8M,5U  
CTRENCH 21 20 22.531P  
CBL 21 20 1.413P  
RX 20 21 1G  
RS 3 21 5.416K  
CWAFAER 21 3 2.587F  
\*extractelement REPORT1 0 REPORTER PARAMS: P0=3.70 P1=4 P3=0 P4=0  
.ENDS PAD4SQ3P7

\*

.SUBCKT DE0172 1 2 21  
CTRENCH 2 202 21.527F  
RFIELDREPI 202 21 446.429  
RREVERT 202 0 1G  
CBL 4 5 19.573F  
RSUB 5 21 82.499K  
CWAFAER 5 21 6.386F

```

CP1EPI 1 4 13.706F
DD 1 4 DCB
RS 4 2 26.809 TC=4.36M,4.344
*extractelement REPORT1 0 REPORTER PARAMS: P0=0 P1=17.20 P2=1 P3=1 P4=1
*extractelement REPORT2 0 REPORTER PARAMS: P0=17.20 P1=4 P2=2.064E-017
*extractelement + P3=0 P4=0 P5=1
.MODEL DCB D( IS=1.514E-018 N=1.050 CJO=41.280F VJ=800M M=500M IBV=1M)
.ENDS DE0172

.PRINT TRAN V(1001) V(1002)
*.PROBE
.END

```

## Circuit Netlist – Output circuit

```

INPUT - MAX3272 OUTPUT CIRCUIT
*
* THIS IS THE TYPICAL CML OUTPUT OF THE MAX3272
*
.OPTIONS ACCT NOMOD NOPAGE LIMPTS=10000 RELTOL=.001
.WIDTH OUT=80
.TEMP 35
* TYPICAL DIE TEMP = 25C + 2.2W*(26C/W) = 80C
.OP
.TRAN 5PS 1500PS
*
* CONVENTIONS VCC = 101, VEE = 102, + OUT = 2000, - OUT = 2002
*
VCC 101 0 DC 3.3
RTERM1 2001 101 100
RTERM2 2002 101 100
RLOAD1 2001 2002 100
CLOAD1 2001 101 0.20P
CLOAD2 2002 101 0.20P
CLOAD3 2001 2002 0.05P

XPK1 2001 2002 1001 1002 0 0 0 OUTPKG
XCIROUT 1001 1002 101 OUTDRV
*
.SUBCKT OUTDRV 71 72 101
VINP 2 0 PULSE (1.25 0.95 0.2N 0.150N 0.150N 0.250N 0.800N)
VINN 3 0 PULSE (0.95 1.25 0.2N 0.150N 0.150N 0.250N 0.800N)
*
RB1 2 22 200
* Adjusted to match waveform of data sheet
RB2 3 32 200
* Adjusted to match waveform of data sheet
*
XQ10 71 22 63 0 N102m066_10
XQ20 72 32 63 0 N102m066_10
*

XRC1 71 101 0 RND50
XRC2 72 101 0 RND50

*
IB1 63 0 16M
*IB2 66 0 4M
*

```

XPAD1 1001 101 PADESD25  
XPAD2 1002 101 PADESD25

\*  
.ENDS OUTDRV  
\*  
\*  
\*\* BEGINNING OF PROCESS LIB  
\*

.SUBCKT PADESD25 1001 101  
XP1 1001 0 PAD4SQ3P7  
XQ1 1001 0 0 DE0172  
XQ2 0 1001 0 DE0172  
.ENDS PADESD25  
\*

.SUBCKT PAD4SQ3P7 1 3  
CPAD 1 10 67.534F  
REPI 10 20 378.507 TC=4.8M,5U  
CTRENCH 21 20 22.531P  
CBL 21 20 1.413P  
RX 20 21 1G  
RS 3 21 5.416K  
CWAFFER 21 3 2.587F  
\*extractelement REPORT1 0 REPORTER PARAMS: P0=3.70 P1=4 P3=0 P4=0  
.ENDS PAD4SQ3P7

\*  
.SUBCKT DE0172 1 2 21  
CTRENCH 2 202 21.527F  
RFIELDDEPI 202 21 446.429  
RREVERT 202 0 1G  
CBL 4 5 19.573F  
RSUB 5 21 82.499K  
CWAFFER 5 21 6.386F  
CP1EPI 1 4 13.706F  
DD 1 4 DCB  
RS 4 2 26.809 TC=4.36M,4.344  
\*extractelement REPORT1 0 REPORTER PARAMS: P0=0 P1=17.20 P2=1 P3=1 P4=1  
\*extractelement REPORT2 0 REPORTER PARAMS: P0=17.20 P1=4 P2=2.064E-017  
\*extractelement + P3=0 P4=0 P5=1  
.MODEL DCB D( IS=1.514E-018 N=1.050 CJO=41.280F VJ=800M M=500M IBV=1M)  
.ENDS DE0172

.SUBCKT RND50 1 2 3  
\*Revision: 1.1 Date: 1999/10/25 16:56:08  
R1 1 4 25 TC=150U  
R2 4 2 25 TC=150U  
C1 1 3 5.388E-016  
C2 4 3 2.155F  
C3 2 3 5.388E-016  
\*XREPORT1 0 REPORTERL1N4  
\*XREPORT2 0 REPORTERL1N5  
\* read ~/lib/gst2/generic/models/resistors/inst\_rnd  
.ENDS RND50

.SUBCKT N102M066\_10 1 2 3 21  
CP1SUB 2 201 15.642F  
RP1SUB 20 201 100K  
CTRENCH 1 202 78.812F  
RFIELDDEPI 202 21 100MEG  
RREVERT 202 20 1M  
CBL 10 20 19.782F  
RSUB 20 21 33.861K  
CWAFFER 20 21 15.558F

```
CP1EPI 10 12 19.174F
CP1P2 12 3 22.114F
RBX 2 12 7.187 TC=1.934M
RCX 1 10 2.032 TC=2.640M,410.600N
RCI 10 11 507.968M TC=2.640M,410.600N
REX 13 3 1.270
QN 11 12 13 11 TX 10
*XREPORT1 0 REPORTERL1N0
*XREPORT2 0 REPORTERL1N1
.MODEL TX NPN( IS=6.926E-018 XTI=3 EG=1.120 BF=380 BR=12 XTB=0 VAF=66
+ VAR=2.500 NF=1.018 NR=1.020 NE=2 NC=1.560 IKF=15.238M IKR=432.900U
+ ISE=3.463E-018 ISC=1.558E-030 RB=17.968 RBM=13.476 IRB=1.558M
+ CJE=16.207F MJE=463M VJE=1.100 FC=990M CJC=7.862F MJC=350M VJC=1
+ TF=1.320P TR=5N XTF=2 VTF=1.200 ITF=56.277M PTF=5 KF=12.979N
+ AF=2.150 )
.ENDS N102M066_10
```

```
.SUBCKT OUTPKG 101 102 201 202 401 402 403
```

```
*
* resistors
```

```
*
RB01 201 301 0.25
RB02 202 302 0.25
```

```
* inductors
```

```
*
LLAP_1_3 101 301 1.2N
LLAP_2_4 102 302 1.3N
K02_03 LLAP_1_3 LLAP_2_4 0.294
```

```
*LB03 PADT PADBOT 23P
```

```
* capacitors
```

```
*
C01 101 403 143F
C02 102 403 143F
```

```
* mutual capacitors
```

```
*
C01_02 101 102 43.800F
.ENDS OUTPKG
```

```
*.PRINT TRAN V(2001) V(2002)
```

```
*.PROBE
```

```
*
.END
```