

MAX3658Aeta and MAX3658Beta I/O Model

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Components*.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

Revision A1, September 07, 2004

Output Model for the MAX3658

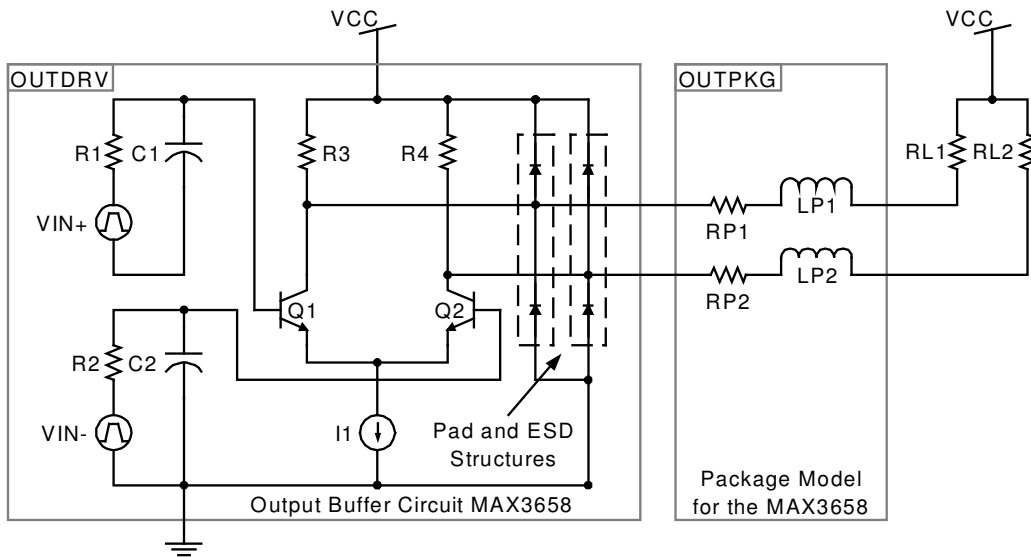


Figure 1. Output Model for signal OUT of the MAX3658.

Notes:

The schematics on the previous page represent the output and input stage of the Maxim MAX3658 622Mbps Transimpedance Amplifier. The output circuit shown is for the signal outputs (OUT+, OUT-). However, the models are given in generic SPICE, which only accepts node names as numbers. As discussed in the application note HFAN 06.3, the output signals are described as (2001, 2002). These models are only valid at 25°C. The bias current for the output circuitry is modeled by ideal current sources. This model is not compensated for variations in VCC, so VCC equal to 3.3V should be used. For die parts, remove the sub-circuit “OUTPKG” and change the load resistance.

The Output Stage: The output stage of the MAX3658 is shown as the sub-circuits “OUTDRV” and “OUTPKG”.

The OUTDRV Sub-circuit: The driver sub-circuit is a simplified version of the output stage used by the MAX3658 Transimpedance Amplifier. The output resistance is 75Ω to VCC. This model is only valid for I_{IN} equal to 2mA. I₁ can be configured to give the desired output amplitude. I₁ equal to 2.008mA gives an output amplitude of 150mVpp. Setting I₁ equal to 3.218mA gives an output amplitude of 240mVpp. Setting I₁ equal to 5.367mA gives an output amplitude of 400mVpp. The waveform is a pulse whose period is 3.2ns. The netlist is given in SPICE 2G6 format in Appendix A.

Text File Format: This model is shipped in “pdf” format. Models and netlists can be copied to text format in the Acrobat Reader by holding the left mouse button on the “Text Select Tool.” Then the user can “select” what netlist and/or subcircuit with the mouse. Then use the copy command from the “edit” menu to capture the selected lines. These lines can then be “pasted” into the user’s text file.

Appendix A: Output Netlist

* 3568 Output Model

.OPT ACCT NOMOD LIMPTS=10000

.TEMP 25

.OP

.TRAN 2P 10n

* Voltage Source

VCC 101 0 3.3

* Load Resistors for packaged parts

RL1 2001 101 75

RL2 2002 101 75

* Load Resistors for die parts

* RL1 50 101 75

* RL2 51 101 75

XOUTPKG 2001 2002 50 51 OUTPKG

XOUTDRV 50 51 101 OUTDRV

.SUBCKT OUTDRV 50 51 101

VINP 1 0 PULSE (1 1.5 0.04n 0.40n 0.40n 1.2n 3.21543n)

VINN 3 0 PULSE (1.5 1 0.04n 0.40n 0.40n 1.2n 3.21543n)

R1 2 1 50

R2 4 3 50

C1 2 0 5p

C2 4 0 5p

* Back Terminated Output Resistors

R3 101 50 75

R4 101 51 75

* Differential Pair

XQ1 50 2 5 0 N102M024_4

XQ2 51 4 5 0 N102M024_4

* For 150mV Differential Output Swing:

* I1 5 0 2.008mA

* For 240mV Differential Output Swing:

* I1 5 0 3.218mA

* For 400mV Differential Output Swing:
I1 5 0 5.367mA

* ESD Diodes
XD1 50 101 0 DE0172
XD2 0 50 0 DE0172
XD3 51 101 0 DE0172
XD4 0 51 0 DE0172

* Pad Structure
XP1 50 0 PAD3SQ3P7
XP2 51 0 PAD3SQ3P7

.ENDS OUTDRV

.SUBCKT OUTPKG 2001 2002 50 51

RP1 50 500 40M
RP2 51 501 40M
LP1 500 2001 .9N
LP2 501 2002 .9N

.ENDS OUTPKG

* Transistor Model
.SUBCKT N102M024_4 1 2 3 21
CP1SUB 2 201 5.199F
RP1SUB 20 201 100K
CTRENCH 1 202 22.907F
RFIELDDEPI 202 21 418.527
RREVERT 202 20 1G
CBL 10 20 4.048F
RSUB 20 21 126.183K
CWAFER 20 21 4.175F
CP1EPI 10 12 4.202F
CP1P2 12 3 4.201F
RBX 2 12 32.509 TC=2.271M
RCX 1 10 11.771 TC=2.717M,449.424N
RCI 10 11 2.943 TC=2.717M,449.424N
REX 13 3 8.599
QN 11 12 13 11 TX 4
.MODEL TX NPN(IS=2.558E-018 XTI=3 EG=1.120 BF=380 BR=12 XTB=0 VAF=66

```
+ VAR=2.500 NF=1.018 NR=1.020 NE=2 NC=1.560 IKF=5.628M IKR=159.900U
+ ISE=1.279E-018 ISC=0 RB=32.509 RBM=24.382 IRB=575.640U CJE=6.016F
+ MJE=463M VJE=1.100 FC=990M CJC=3.276F MJC=350M VJC=1 TF=1.320P
TR=5N
+ XTF=2 VTF=1.200 ITF=20.787M PTF=5 KF=102.378N AF=2.150 )
.ENDS N102M024_4
```

```
* Diode Model
.SUBCKT DE0172 1 2 21
CTRENCH 2 202 21.527F
RFIELDDEPI 202 21 446.429
RREVERT 202 20 1G
CBL 4 5 19.573F
RSUB 5 21 82.499K
CWAFFER 5 21 6.386F
CP1EPI 1 4 13.706F
DD 1 4 DCB
RS 4 2 26.809 TC=4.361M,4.344U
.MODEL DCB D( IS=1.514E-018 N=1.050 CJO=41.280F VJ=800M M=500M )
.ENDS DE0172
```

```
* Pad Model
.SUBCKT PAD3SQ3P7 1 3
CPAD 1 10 99.132F
REPI 10 20 396.030 TC=4.800M,5U
CTRENCH 21 20 22.531F
CBL 21 20 1.413P
RX 20 21 1G
RS 3 21 5.416K
CWAFFER 21 3 2.587F
.ENDS PAD3SQ3P7
```

```
.PROBE
.END
```