MAX3748 I/O Model
Multi-Rate Limiter

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Component*s.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

I/O Models for the MAX3748 Multirate Limiter

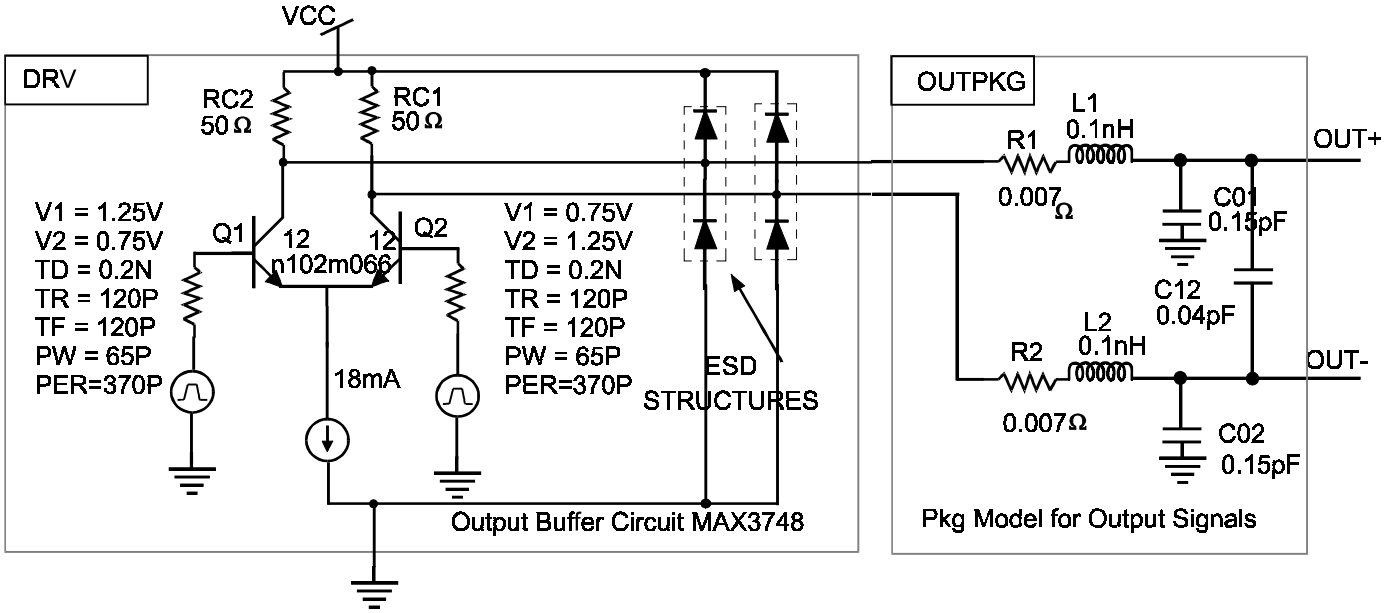

Figure 1. Output signal buffer for the MAX3748 including a simplified package model.

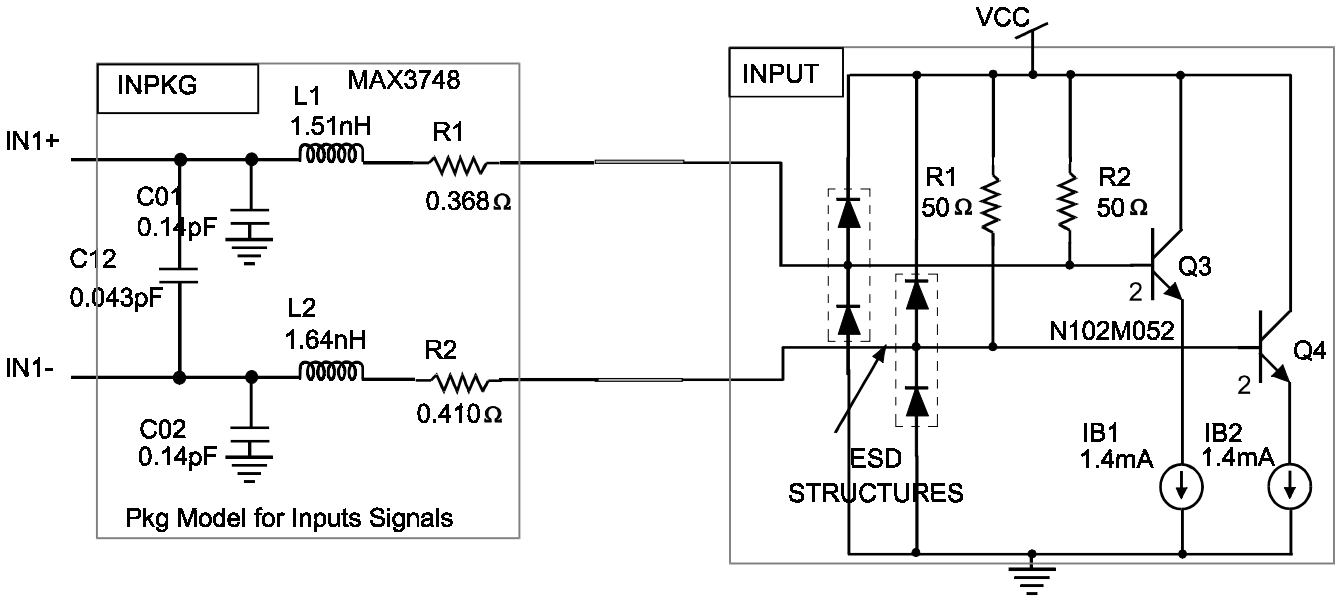

Figure 2. Simplified input package model and input circuitry for the MAX3804

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MAX3748 Multi-Rate Limiter

Notes:

The schematics on the previous page represent the output and input stage of the Maxim MAX3748 10Gbps equalizer. The output circuit shown is for the signal outputs (OUT+, OUT-). However the models are given in generic SPICE which only accepts node names as numbers. As discussed in the application note the signals are described as (2001, 2002). Similarly for the input stage.

The Output Stage: The output stage of the MAX3804 is shown as two sub-circuits “DRV” and “OUTPKG.” The sub-circuit DRV is a model of the circuitry on chip and the OUTPKG is a very simple model of the package. The package is for flipchip die, so there is little series inductance and resistance.

The DRV Driver Sub-circuit: The output stage is consists of a signal source driving a differential pair. The collectors are connected to 50 Ohm resistors tied to $V_{CC.}$ The signals at the collectors are connected to the output pads.

The Input Stage: The input stage is comprised of two subcircuits INPKG and INPUT. The previous comments of the output stage above apply equally to the input network.

Appendix A: Circuit Schematic for Input/Output Circuitry (MAX3748) with Simplified Package Model

Circuit Netlist – Input Circuit - SPICE

```
INPUT - MAX3748 INPUT CIRCUIT
*
* This example is the input circuit for the MAX3748
*
.OPT ACCT NOMOD NOPAGE RELTOL=.001 LIMPTS=1001

.WIDTH OUT=80

* TEMP = 27 + 115mW/17.1 = 34
.TEMP 34
.OP
.TRAN 2PS 600PS
VCC 101 0 DC 3.3

VINA 2 0 PULSE (3.3 2.5 0.05n 0.030n 0.030n 0.075n 0.20n)
VINB 3 0 PULSE (2.5 3.3 0.05n 0.030n 0.030n 0.075n 0.20n)
RLOAD1 2 1001 50
CLOAD1 101 1001 0.02p
RLOAD2 3 1002 50
CLOAD2 101 1002 0.02p

XPK1 1001 1002 8 9 INPKG

XCIROUT 8 9 101 INPUT

.SUBCKT INPUT 3001 3002 101

* The power supplly is 3.3Volts.

XQ3 101 3001 4 0 n102m066_2
XQ4 101 3002 5 0 N102M066_2

IB1 4 0 1.40M
IB2 5 0 1.40M

R1 101 3001 50
R2 101 3002 50

.ENDS INPUT

*
.SUBCKT INPKG 401 402 501 502
*
* resistors
*
RB01 501 601 .007M
RB02 502 602 .007M
*
* inductors
*
LLAP_1_3 401 601 0.1N
LLAP_2_4 402 602 0.1N

*
* capacitors
*
C01 401 0 150F
C02 402 0 150F
*
```

```
* mutual capacitors
*
C01_02 401 402 40F
.ENDS INPKG


.SUBCKT DE0172 1 2 21
CTRENCH 2 202 21.527F
RFIELDEPI 202 21 446.429
RREVERT 202 21 1G
CBL 4 5 19.573F
RSUB 5 21 82.499K
CWAFER 5 21 6.386F
CP1EPI 1 4 13.706F
DD 1 4 DCB
RS 4 2 26.809 TC=4.361M,4.344U
*XREPORT1 0 REPORTERL1N25
*XREPORT2 0 REPORTERL1N26
.MODEL DCB D( IS=1.514E-018 N=1.050 CJO=41.280F VJ=800M M=500M )
.ENDS DE0172
.SUBCKT PADESD25 2 3 4 5
XP1 2 5 PAD4SQ3P7
XQ1 2 3 5 DE0172
XQ2 4 2 5 DE0172
.ENDS PADESD25

.SUBCKT PAD4SQ3P7 1 3
CPAD 1 10 67.534F
REPI 10 20 378.507 TC=4.800M,5U
CTRENCH 21 21 22.531F
CBL 21 20 1.413P
RX 20 21 1G
RS 3 21 5.416K
CWAFER 21 3 2.587F
*XREPORT1 0 REPORTERL1N35
.ENDS PAD4SQ3P7

*
.SUBCKT N102M066_2 1 2 3 21
CP1SUB 2 201 18.770F
RP1SUB 20 201 100K
CTRENCH 1 202 94.575F
RFIELDEPI 202 21 101.461
RREVERT 202 20 1G
CBL 10 20 23.739F
RSUB 20 21 28.218K
CWAFER 20 21 18.670F
CP1EPI 10 12 23.008F
CP1P2 12 3 26.536F
RBX 2 12 5.989 TC=1.934M
RCX 1 10 1.693 TC=2.640M,410.600N
RCI 10 11 423.307M TC=2.640M,410.600N
REX 13 3 1.059
QN 11 12 13 11 TX 12
*XREPORT1 0 REPORTERL1N11
*XREPORT2 0 REPORTERL1N12
.MODEL TX NPN( IS=6.926E-018 XTI=3 EG=1.120 BF=380 BR=12 XTB=0 VAF=66
+   VAR=2.500 NF=1.018 NR=1.020 NE=2 NC=1.560 IKF=15.238M IKR=432.900U
+   ISE=3.463E-018 ISC=1.558E-030 RB=17.968 RBM=13.476 IRB=1.558M
+   CJE=16.207F MJE=463M VJE=1.100 FC=990M CJC=7.862F MJC=350M VJC=1
+   TF=1.320P TR=5N XTF=2 VTF=1.200 ITF=56.277M PTF=5 KF=10.524N
+   AF=2.150 )
.ENDS N102M066_2

.PRINT TRAN  V(1001) V(1002)
*.PROBE
.END
```

Circuit Netlist – Output Circuit – SPICE

```
INPUT - MAX3748 OUTPUT CIRCUIT

.OPT ACCT NOMOD NOPAGE RELTOL=.001 LIMPTS=1001

* TEMP = 27 + 115mW/17.1 =38
.TEMP 38
.OP
.TRAN 5PS 1500PS

VCC 101 0 DC 3.3
RLOAD1 2001 101 50
RLOAD2 2002 101 50
CLOAD1 2001 101 0.20PF
CLOAD2 2002 101 0.20PF
CLOAD3 2001 2002 0.05pF
XPK1 2001 2002 4 5 0 0 0 OUTPKG
XCIROUT 4 5 101 DRV

.SUBCKT DRV 1001 1002 101

*VINP 2 0 PULSE (1.25 0.95 0.05n 0.010n 0.010n 0.080n 0.20n)
*VINN 3 0 PULSE (0.95 1.25 0.05n 0.020n 0.020n 0.080n 0.20n)
VINP 2 0 PULSE (1.25 0.75 0.2n 0.080n 0.080n 0.220n 0.600n)
VINN 3 0 PULSE (0.75 1.25 0.2n 0.080n 0.080n 0.220n 0.600n)


RB1 2 22 200
RB2 3 32 200

XQ1 1001 22 61 0 n102m066_12
XQ2 1002 32 61 0 n102m066_12

RC1 1001 101 50
RC2 1002 101 50


IB1 61 0 18.0M
XPAD1 1001 101 0 0 PADESD25
XPAD2 1002 101 0 0 PADESD25

.ENDS DRV

.SUBCKT N102M066_12 1 2 3 21
CP1SUB 2 201 18.770F
RP1SUB 20 201 100K
CTRENCH 1 202 94.575F
RFIELDEPI 202 21 101.461
RREVERT 202 20 1G
CBL 10 20 23.739F
RSUB 20 21 28.218K
CWAFER 20 21 18.670F
CP1EPI 10 12 23.008F
CP1P2 12 3 26.536F
RBX 2 12 5.989 TC=1.934M
RCX 1 10 1.693 TC=2.640M,410.600N
RCI 10 11 423.307M TC=2.640M,410.600N
REX 13 3 1.059
QN 11 12 13 11 TX 12
*XREPORT1 0 REPORTERL1N11
*XREPORT2 0 REPORTERL1N12
.MODEL TX NPN( IS=6.926E-018 XTI=3 EG=1.120 BF=380 BR=12 XTB=0 VAF=66
```

```
+   VAR=2.500 NF=1.018 NR=1.020 NE=2 NC=1.560 IKF=15.238M IKR=432.900U
+   ISE=3.463E-018 ISC=1.558E-030 RB=17.968 RBM=13.476 IRB=1.558M
+   CJE=16.207F MJE=463M VJE=1.100 FC=990M CJC=7.862F MJC=350M VJC=1
+   TF=1.320P TR=5N XTF=2 VTF=1.200 ITF=56.277M PTF=5 KF=10.524N
+   AF=2.150 )
.ENDS N102M066_12

.SUBCKT DE0172 1 2 21
CTRENCH 2 202 21.527F
RFIELDEPI 202 21 446.429
RREVERT 202 21 1G
CBL 4 5 19.573F
RSUB 5 21 82.499K
CWAFER 5 21 6.386F
CP1EPI 1 4 13.706F
DD 1 4 DCB
RS 4 2 26.809 TC=4.361M,4.344U
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*XREPORT2 0 REPORTERL1N26
.MODEL DCB D( IS=1.514E-018 N=1.050 CJO=41.280F VJ=800M M=500M )
.ENDS DE0172

.SUBCKT PADESD25 2 3 4 5
XP1 2 5 PAD4SQ3P7
XQ1 2 3 5 DE0172
XQ2 4 2 5 DE0172
.ENDS PADESD25

.SUBCKT PAD4SQ3P7 1 3
CPAD 1 10 67.534F
REPI 10 20 378.507 TC=4.800M,5U
CTRENCH 21 21 22.531F
CBL 21 20 1.413P
RX 20 21 1G
RS 3 21 5.416K
CWAFER 21 3 2.587F
*XREPORT1 0 REPORTERL1N35
.ENDS PAD4SQ3P7


.SUBCKT OUTPKG 101 102 201 202 401 402 403
*
* resistors
*
RB01 201 301 0.007
RB02 202 302 0.007
*
* inductors
*
LLAP_1_3 101 301 0.1N
LLAP_2_4 102 302 0.1N

*LB03 PADT PADBOT 23P
*
* capacitors
*
C01 101 403 150F
C02 102 403 150F
*
* mutual capacitors
*
C01_02 101 102 40F
.ENDS OUTPKG

.PRINT TRAN V(2001) V(2002)
*.PROBE

.END
```