

MAX3750 I/O Model

SPICE I/O Macromodels aid in understanding signal integrity issues in electronic systems. Most of Maxim's High Frequency/Fiber Communication ICs utilize input and output (I/O) circuits with Current Mode Logic (CML), Positive Emitter Coupled Logic (PECL), and Low Voltage Differential Signal (LVDS) formats to transfer data into and out of an IC. These models are based on simplified circuit expressions that may include replacement of active circuit elements with ideal controlled voltage and current sources. As such, simulation with macromodels should be treated as 'typical' performance and not relied upon as final proof-of-design. Use of macromodel descriptions is not a substitute for worst-case design analysis, nor for testing real circuits over temperature, supply, and other operating limits.

The output format is provided as ASCII text netlists suitable for generic SPICE. This format is compatible with most versions of SPICE such as PSPICE and HSPICE. Additional information is found in HFAN 6.1 *Input/Output Models for Maxim Fiber Components*.

To extract the circuit netlists using the Adobe Acrobat Reader follow these instructions. Select the "Text Select Tool" by clicking the left mouse button on this icon of the menu bar (a capital T with a small dashed box to the lower right). Highlight the desired netlist text with the cursor. Use the copy command from the edit menu to capture the selected lines. Then paste the selected lines into a text file editor and save the file with an extension compatible with the simulator.

Revision A, March 3, 03

Revision A1, May 18, 02

I/O Models for the MAX3750 Dual Rate Fibre Receivers

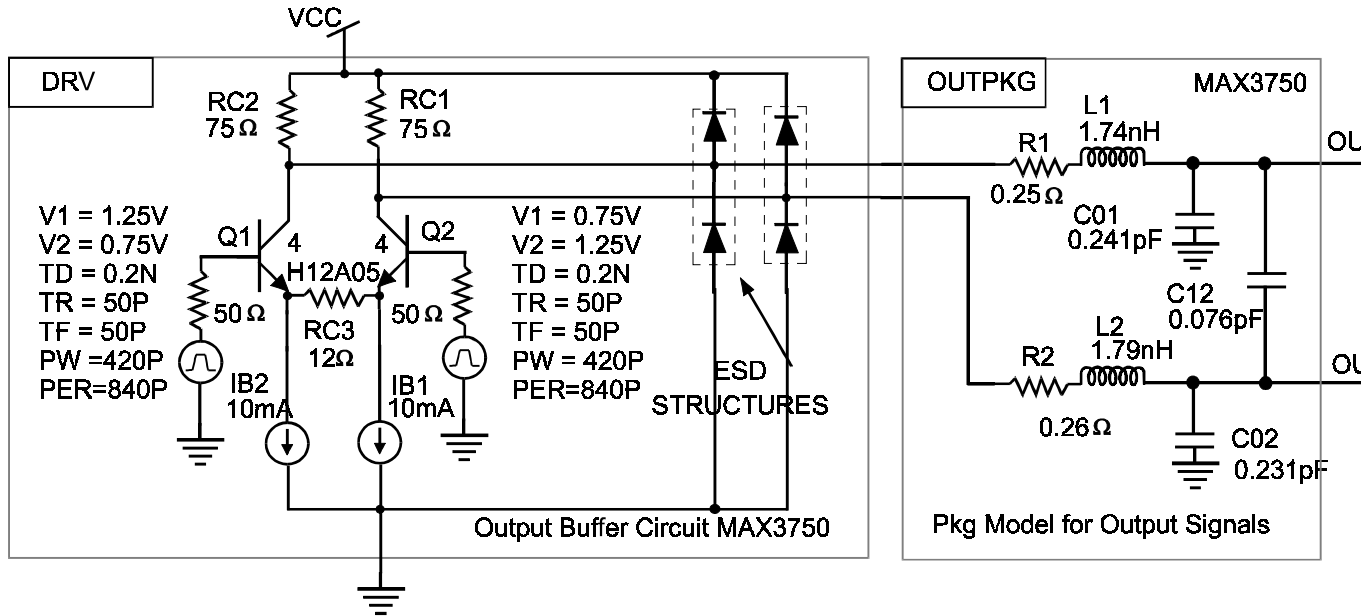


Figure 1. Output signal buffer for the MAX3750 including a simplified package model. The model for LOUT- is approximately equal to the OUT- model.

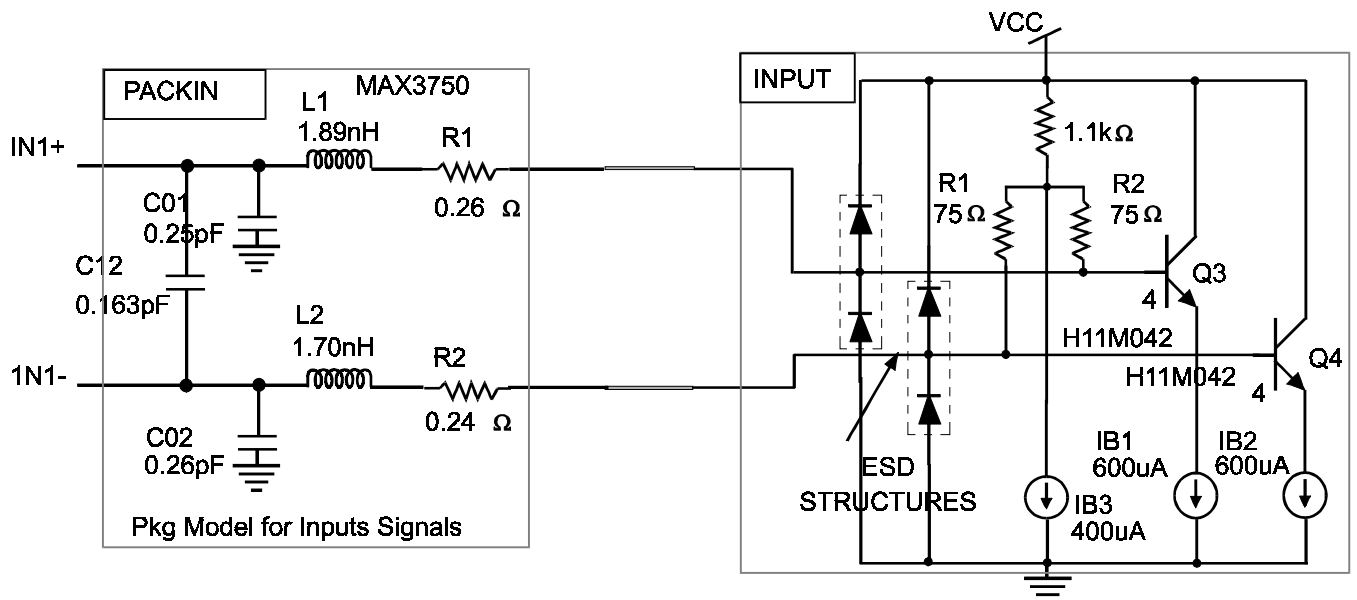


Figure 2. Simplified input package model and input circuitry for the MAX3750. The input model for LN+ is approximately equal to the IN+ model.

Notes:

The schematics on the previous page represent the output and input stage of the Maxim MAX3750 Dual rate Fiber channel repeater. The output circuit shown is for the signal outputs (OUT+, OUT-). However the models are given in generic SPICE which only accepts node names as numbers. As discussed in the application note the signals are described as (2001, 2002). Similarly for the input stage.

The Output Stage: The output stage of the MAX3780 is shown as two sub-circuits “DRV” and “OUTPKG.” The sub-circuit DRV is a model of the circuitry on chip and the OUTPKG is a very simple model of the package.

The DRV Driver Sub-circuit: The bias currents in both input and output circuitry are modeled by current sources. The signal sources in the output stage are modeled by ideal voltage generators whose signal swings are from 0.75 to 1.25 Volts. The waveform is a pulse whose period is 470ps. The ESD structure is modeled by a .490pF capacitance. The output driver transistor Q1 is actually implemented by 5 H12A05 transistors in parallel. In Appendix A the netlist is given in SPICE 2G6 format. In this netlist the transistor model H12A05_4 has been scaled by a factor of four for the simple simulator used as the actual circuit uses the five transistors in parallel. The settings of IE1 = IE2 = 10mA and RC3 = 12 Ω provide an output signal swing of about 1400mV_{p-p}. To lower the output signal swing to 200mV_{p-p}, increase RC3 to 25 Ω and lower the settings of IE1=IE2=6 mA. To increase the signal swing to 2200mV_{p-p} use RC3 = 12 Ω and IE1=IE2= 15 mA.

The OUTPKGPackage Subcircuit: Each output signal in the package subcircuit is modeled as an r-l-c network, which each output capacitively coupled to each other. A simple inductor and a stray capacitance to ground have modeled the bond wire. This network has a significant effect on the shape of the output signal. This simple model is listed in the output netlist. This simplistic model for the package does not include the mutual inductance to the adjacent bondwires. The skin loss resistance of the bondwire with frequency is modeled. For the netlist of the simple package model the skin loss was evaluated at 2.1GHz.

The Input Stage: The input stage is comprised of two subcircuits PACKIN and INPUT. The previous comments of the output stage above apply equally to the input network.

Text File Format: This model is shipped in “pdf” format. Models and netlists can be copied to text format in the Acrobat Reader by holding the left mouse button on the “Text Select Tool.” Then the user can “select” what netlist and/or subcircuit with the mouse. Then use the copy command from the “edit” menu to capture the selected lines. These lines can then be “pasted” into the user’s text file.

Appendix A: Circuit Schematic for Input/Output Circuitry (MAX3750) with Simplified Package Model

Circuit Netlist – Input Circuit – SPICE

```
INPUT - MAX3750 INPUT CIRCUIT

*

* This example is the input circuit for the MAX3750

*

.OPT ACCT NOMOD NOPAGE RELTOL=.001 LIMPTS=1001

.WIDTH OUT=80

* TEMP = 27 + 290mW/18.9 = 42

.TEMP 42

.OP

.TRAN 5PS 1.3NS

VCC 101 0 DC 3.3

VINA 2 0 PULSE (3.3 2.5 0.2n 0.050n 0.050n 0.370n 0.840n)

VINB 3 0 PULSE (2.5 3.3 0.2n 0.050n 0.050n 0.370n 0.840n)

RLOAD1 2 1001 75

CLOAD1 101 1001 0.2p

RLOAD2 3 1002 75

CLOAD2 101 1002 0.2p

CLOAD3 1001 1002 0.05p

XPK1 1001 1002 8 9 PACKIN

XCIROUT 8 9 101 INPUT

.SUBCKT INPUT 3001 3002 101

* The power supply is 3.3Volts.

XQ3 101 3001 4 0 H11M042_4
```

XQ4 101 3002 5 0 H11M042_4

R1 1 3001 75

R2 1 3002 75

R3 1 101 1200

C1 1 101 .50pF

IB1 4 0 0.20M

IB2 5 0 0.20M

IB3 1 0 0.40M

XPAD1 3001 0 HPAD3

XPAD2 3002 0 HPAD3

XESD1 3001 101 0 HDE113032

XESD2 0 3001 0 HDE113032

XESD3 3002 101 0 HDE113032

XESD4 0 3002 0 HDE113032

*CESD1 3001 0 .490P

*CESD2 3002 0 .490P

.ENDS INPUT

*

.SUBCKT PACKIN 401 402 501 502

*

* resistors

*

RB01 501 601 .26M

RB02 502 602 .25M

*

* inductors

*

LLAP_1_3 401 601 1.89N

LLAP_2_4 402 602 1.70N

*KLAP_1_2 LLAP_1_3 LLAP_2_4 0.364466

*LB03 PADT PADBOT 23P

*

* capacitors

*

C01 401 0 246F

C02 402 0 237F

*

* mutual capacitors

*

C01_02 401 402 79.800F

.ENDS PACKIN

.SUBCKT HPAD3 1 3

CPAD 1 10 86.407F

REPI 10 20 149.204M TC=4.800M,5U

CTRENCH 21 20 79.795F

DS 21 20 DSUB

RS 3 21 369.115

*XREPORT1 0 REPORTERL1N94

.MODEL DSUB D(IS=98.719F CJO=555.750F M=400M VJ=650M)

.ENDS HPAD3

.SUBCKT H11M042_4 1 2 3 21

CP1EPI 1 2 7.178F

CP1P2 12 3 19.725F

CTRENCH 1 20 26.787F
 RBX 2 12 24.116 TC=2.417M
 RCX 1 10 13.647 TC=2.996M,1.687U
 RCI 10 11 718.283M TC=2.996M,1.687U
 REX 13 3 2.631 TC=56.308U
 RSUB 20 21 4.155K
 QP 20 10 12 20 TXP 4 OFF
 QN 11 12 13 11 TX 4
 *XREPORT1 0 REPORTERL1N11
 *XREPORT2 0 REPORTERL1N12
 .MODEL TX NPN(IS=8.314E-018 XTI=3 EG=1.140 BF=232.533 BR=20 XTB=450M
 + VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=31.636M
 + IKR=579.600U ISE=3.932E-021 ISC=5.056E-030 RB=96.463 RBM=72.347
 + IRB=5.056M CJE=26.918F MJE=490M VJE=940M FC=990M CJC=5.482F MJC=470M
 + VJC=850M TF=3.778P TR=19N XTF=1 VTF=1K ITF=14.905M PTF=5 KF=1.500F
 + AF=1)
 .MODEL TXP PNP(IS=4.920E-019 CJE=5.482F MJE=470M VJE=850M CJC=6.613F
 + MJC=400M VJC=650M BF=10K BR=884.918U TF=1N FC=900M)
 .ENDS H11M042_4

 .SUBCKT HDE113032 1 2 21
 CP1EPI 1 4 88.881F
 QD 5 4 1 5 QESD
 RS 4 2 2.531 TC=2.729M,1.896U
 RSUB 5 21 2.936K
 CTRENCH 2 5 22.961F
 *XREPORT1 0 REPORTERL1N66
 *XREPORT2 0 REPORTERL1N67
 .MODEL QESD PNP(IS=1.181E-017 NF=1.050 BF=800M BR=600U CJE=155.018F

+ VJE=600M MJE=400M CJC=53.258F VJC=650M MJC=400M)

.ENDS HDE113032

.PRINT TRAN V(1001) V(1002)

*.PROBE

.END

Circuit Netlist – Output Circuit — SPICE

INPUT - MAX3750 OUTPUT CIRCUIT

.OPT ACCT NOMOD NOPAGE RELTOL=.001 LIMPTS=1001

* TEMP = 27 + 290mW/18.1 = 42

.TEMP 42

.OP

.TRAN 5PS 1500PS

VCC 101 0 DC 3.3

RLOAD1 2001 101 75

RLOAD2 2002 101 75

CLOAD1 2001 101 0.20PF

CLOAD2 2002 101 0.20PF

CLOAD3 2001 2002 0.05pF

XPK1 2001 2002 4 5 0 0 0 OUTPKG

XCIROUT 4 5 101 DRV

.SUBCKT DRV 1001 1002 101

VINP 2 0 PULSE (1.25 0.95 0.2n 0.050n 0.050n 0.370n 0.840n)

VINN 3 0 PULSE (0.95 1.25 0.2n 0.050n 0.050n 0.370n 0.840n)

RB1 2 22 50

RB2 3 32 50

XQ1 1001 22 61 0 H12A05_4

XQ2 1002 32 62 0 H12A05_4

RC1 1001 101 75

RC2 1002 101 75

IB1 61 0 10.0M

IB2 62 0 10.0M

RC3 61 62 12

XPAD1 1001 0 HPAD3

XPAD2 1002 0 HPAD3

XESD1 1001 101 0 HDE113032

XESD2 0 1001 0 HDE113032

XESD3 1002 101 0 HDE113032

XESD4 0 1002 0 HDE113032

.ENDS DRV

.SUBCKT H12A05_4 1 2 3 21

CP1EPI 1 2 28.590F

CP1P2 12 3 51.660F

CTRENCH 1 20 42.094F

RBX 2 12 7.635 TC=2.649M

RCX 1 10 8.967 TC=2.315M,931.161N

RCI 10 11 471.963M TC=2.315M,931.161N

REX 13 3 1.082 TC=182.441U

RSUB 20 21 2.252K

QP 20 10 12 20 TXP 4 OFF

QN 11 12 13 11 TX 4

```

*XREPORT1 0 REPORTERL1N33
*XREPORT2 0 REPORTERL1N34
.MODEL TX NPN( IS=2.302E-017 XTI=3 EG=1.140 BF=223.719 BR=20 XTB=450M
+ VAF=29 VAR=3.500 NF=1.010 NR=1.020 NE=1.650 NC=1.560 IKF=88.032M
+ IKR=1.613M ISE=1.089E-020 ISC=1.400E-029 RB=30.538 RBM=22.904
+ IRB=14M CJE=74.302F MJE=490M VJE=940M FC=990M CJC=14.718F MJC=470M
+ VJC=850M TF=3.814P TR=19N XTF=1 VTF=1K ITF=40.860M PTF=5 KF=1.500F
+ AF=1 )
.MODEL TXP PNP( IS=1.308E-018 CJE=14.718F MJE=470M VJE=850M CJC=13.849F
+ MJC=400M VJC=650M BF=10K BR=869.864U TF=1N FC=900M )
.ENDS H12A05_4

```

```

.SUBCKT HPAD3 1 3
CPAD 1 10 86.407F
REPI 10 20 149.204M TC=4.800M,5U
CTRENCH 21 20 79.795F
DS 21 20 DSUB
RS 3 21 369.115

```

```

*XREPORT1 0 REPORTERL1N94
.MODEL DSUB D( IS=98.719F CJO=555.750F M=400M VJ=650M )
.ENDS HPAD3

```

```

.SUBCKT HDE113032 1 2 21
CP1EPI 1 4 88.881F
QD 5 4 1 5 QESD
RS 4 2 2.531 TC=2.729M,1.896U
RSUB 5 21 2.936K
CTRENCH 2 5 22.961F
*XREPORT1 0 REPORTERL1N66
*XREPORT2 0 REPORTERL1N67
.MODEL QESD PNP( IS=1.181E-017 NF=1.050 BF=800M BR=600U CJE=155.018F
+ VJE=600M MJE=400M CJC=53.258F VJC=650M MJC=400M )
.ENDS HDE113032

```

```

.SUBCKT OUTPKG 101 102 201 202 401 402 403

```

```

*
* resistors
*
RB01 201 301 0.25
RB02 202 302 0.25

```

```

* inductors
*
LLAP_1_3 101 301 1.79N
LLAP_2_4 102 302 1.74N

```

```

*LB03 PADT PADBOT 23P

```

```

*
* capacitors
*
C01 101 403 241F
C02 102 403 231F

```

```

* mutual capacitors
*
C01_02 101 102 75.800F
.ENDS OUTPKG

```

.PRINT TRAN V(2001) V(2002)

*.PROBE

.END